Advanced Backplane Circuits Data Book

TEXAS INSTRUMENTS

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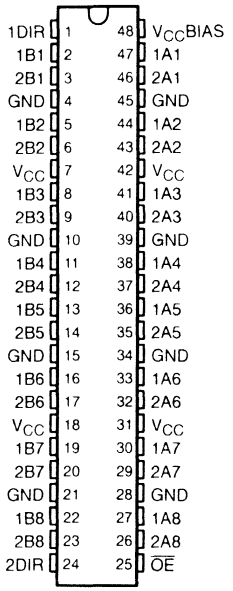
CONTENTS

Texas Instruments has developed Enhanced Transceiver Logic (ETL) devices designated ABTE that are compatible with the ETL standard. By using these devices, the performance and functionality of VME and proprietary TTL backplanes can be improved. Fully backward compatible with TTL, the ETL transceivers offer a narrower switching region, improved noise margins, live insertion, bushold on inputs, series damping resistors on high-drive outputs, and space-saving package options.

- Supports the VME64 ETL Specification
- Reduced, TTL-Compatible, Input Threshold Range
- High-Drive Outputs (I_{OH} = –60 mA, I_{OL} = 90 mA) Support 25-Ω Incident-Wave Switching
- V_{CC}BIAS Pin Minimizes Signal Distortion During Live Insertion
- Internal Pullup Resistor on $\overline{OE}$ Keeps Outputs in High-Impedance State During Power Up or Power Down
- Members of the Texas Instruments *Widebus*™ Family
- State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- 25-Ω Series Dampening Resistor on B Port
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-Mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54ABTE16245 . . . WD PACKAGE
SN74ABTE16245 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The 'ABTE16245 are 16-bit (dual-octal) noninverting 3-state transceivers designed for synchronous two-way communication between data buses. The control function implementation minimizes external timing requirements. These devices can be used as two 8-bit transceivers or one 16-bit transceiver. They allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated.

The B port has a 25-Ω series output resistor to reduce ringing. Active bus-hold inputs are also found on the B port to hold unused or floating inputs at a valid logic level.

The A port provides for the precharging of the outputs via V_{CC}BIAS, which establishes a voltage between 1.3 V and 1.7 V when V_{CC} is not connected.

The SN74ABTE16245 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABTE16245 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABTE16245 is characterized for operation from –40°C to 85°C.

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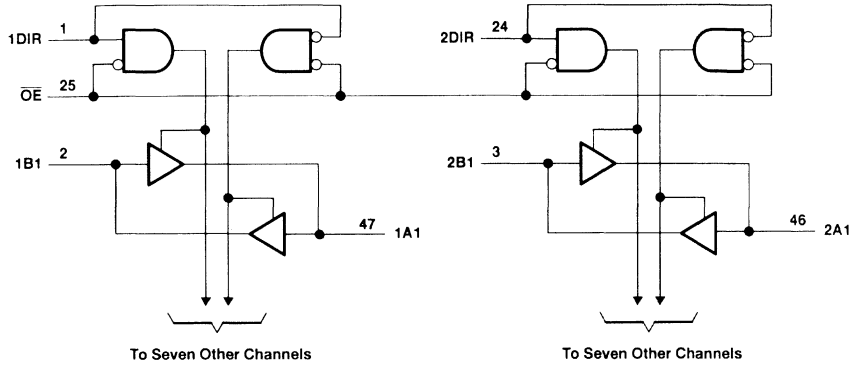
TEXAS INSTRUMENTS

FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	A data to B bus
L	H	B data to A bus
H	X	Isolation

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DGG package ..... 0.85 W
DL package ..... 1.2 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 3)

			SN54ABTE16245			SN74ABTE16245			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	$\overline{OE}$	2			2			V
		Except $\overline{OE}$	1.6			1.6			
V_{IL}	Low-level input voltage	$\overline{OE}$			0.8			0.8	V
		Except $\overline{OE}$			1.4			1.4	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	B bus			−12			−12	mA
		A bus			−24			−60	
I_{OL}	Low-level output current	B bus			12			12	mA
		A bus			64			90	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10			10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 3: Unused or floating pins (input or A-bus I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ABTE16245			SN74ABTE16245			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V, I_I = −18 mA				−1.2			−1.2	V
V_{OH}	B port	V_{CC} = 5.5 V, I_{OH} = − 100 µA				V_{CC}−0.2			V_{CC}−0.2	V
		V_{CC} = 4.5 V	I_{OH} = − 1 mA	2.4			2.4			
			I_{OH} = − 12 mA	2			2			
	A port	V_{CC} = 5.5 V, I_{OH} = − 1 mA				4.5			4.5	
		V_{CC} = 4.5 V	I_{OH} = − 32 mA	2.4			2.4			
			I_{OH} = − 64 mA				2			
V_{OL}	B port	V_{CC} = 4.5 V	I_{OL} = 1 mA			0.4			0.4	V
			I_{OL} = 12 mA						0.8	
	A port	V_{CC} = 4.5 V	I_{OL} = 64 mA			0.55			0.55	
			I_{OL} = 90 mA						0.9	
$I_{I(hold)}$	B port	V_{CC} = 4.5 V	V_I = 0.8 V	100			100			µA
			V_I = 2 V	−100			−100			
		V_{CC} = 5.5 V, V_I = 0 to 5.5 V				±500			±500	
I_I	Control inputs	V_{CC} = 5.5 V, V_I = V_{CC} or GND				±1			±1	µA
	A or B ports	V_{CC} = 5.5 V, V_I = V_{CC} or GND				±20			±20	
I_{OZH}‡	A port	V_{CC} = 5.5 V, V_O = 2.7 V				10			10	µA
I_{OZL}‡	A port	V_{CC} = 5.5 V, V_O = 0.5 V				−10			−10	µA
I_O	A port	V_{CC} = 5.5 V, V_O = 0		−50	−120	−180	−50		−180	µA
	B port			−25	−52	−90	−25		−90	
I_{off}		V_{CC} = 0, V_I or V_O ≤ 4.5 V, V_{CC}BIAS = 0				±100			±100	µA
I_{CC}	A or B ports	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high		28	36		28	36	mA
			Outputs low		38	48		38	48	
			Outputs disabled		20	32		20	32	
I_{CCD}	A or B ports	V_{CC} = 5 V, C_L = 50 pF	$\overline{OE}$ high		0.02			0.02		mA/ MHz
			$\overline{OE}$ low		0.33			0.33		
C_i	Control inputs	V_I = 2.5 V or 0.5 V			2.5	4		2.5	4	pF
C_{io}	I/O ports	V_O = 2.5 V or 0.5 V			4.5	8		4.5	8	pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.

live-insertion specifications over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS	SN54ABTE16245			SN74ABTE16245			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
I_{CC} (V_{CC}BIAS)		V_{CC} = 0 to 4.5 V, V_{CC}BIAS = 4.5 V to 5.5 V, $I_{O(DC)}$ = 0		250	700		250	700	μA
		V_{CC} = 4.5 V to 5.5 V‡, V_{CC}BIAS = 4.5 V to 5.5 V, $I_{O(DC)}$ = 0			20			20	
V_O	A port	V_{CC} = 0, V_{CC}BIAS = 4.5 V to 5.5 V	1.1	1.5	1.9	1.1	1.5	1.9	V
		V_{CC} = 0, V_{CC}BIAS = 4.75 V to 5.25 V	1.3	1.5	1.7	1.3	1.5	1.7	
I_O	A port	V_{CC} = 0, V_O = 0, V_{CC}BIAS = 4.5 V	−20		−100	−20		−100	μA
		V_{CC} = 0, V_O = 3 V, V_{CC}BIAS = 4.5 V	20		100	20		100	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ V_{CC} – 0.5 V < V_{CC}BIAS

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABTE16245		SN74ABTE16245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1.5	3.3	4.2	1.5	5.4	1.5	5.2	ns
t_{PHL}			1.5	3.8	4.6	1.5	5.4	1.5	5.2	
t_{PLH}	B	A	1.5	3	3.8	1.5	4.7	1.5	4.5	ns
t_{PHL}			1.5	3.1	4	1.5	4.7	1.5	4.5	
t_{PZH}	$\overline{OE}$	A	2	3.9	5.3	2	6.4	2	6.2	ns
t_{PZL}			2	4.4	5.9	2	7	2	6.8	
t_{PZH}	$\overline{OE}$	B	2	4.5	6	2	7.3	2	7.1	ns
t_{PZL}			2	5	6.4	2	7.5	2	7.3	
t_{PHZ}	$\overline{OE}$	A	2	4.9	5.9	2	7	2	6.7	ns
t_{PLZ}			2	3.7	4.6	2	5.4	2	5.1	
t_{PHZ}	$\overline{OE}$	B	2	5.2	6.2	2	7.2	2	7	ns
t_{PLZ}			2	4	5	2	5.8	2	5.5	

extended switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Note 4 and Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD	V_{CC} = 5 V, T_A = 25°C			SN54ABTE16245		SN74ABTE16245		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	B	A	R_X = 13 Ω	1.5	3.2	4	1.5	5	1.5	4.8	ns
t_{PHL}				1.5	3.8	4.7	1.5	5.8	1.5	5.6	
t_{PLH}	B	A	R_X = 26 Ω	1.5	3.1	4	1.5	4.8	1.5	4.6	ns
t_{PHL}				1.5	3.5	4.4	1.5	5.2	1.5	4.9	
t_{PLH}	B	A	R_X = 56 Ω	1.5	3	3.8	1.5	4.7	1.5	4.5	ns
t_{PHL}				1.5	3.3	4.2	1.5	5.1	1.5	4.7	
$t_{sk(p)}$	B	A	R_X = Open		0.1	0.6		2		2	ns
	A	B			0.4	0.8		2		2	
	B	A	R_X = 26 Ω		0.3	0.8		2		2	
$t_{sk(o)}$	B	A	R_X = Open		0.3	0.7		1.3		1.3	ns
	A	B			0.7	1.1		1.3		1.3	
	B	A	R_X = 26 Ω		0.5	1		1.3		1.3	
t_t†	B	A	R_X = 26 Ω	0.5	0.8	1.5	0.5	1.5	0.5	1.5	ns
t_t‡	A	B	Rise or fall time 10%–90%	3.5	5.5	7.3	3.5	8.1	3.5	7.9	ns

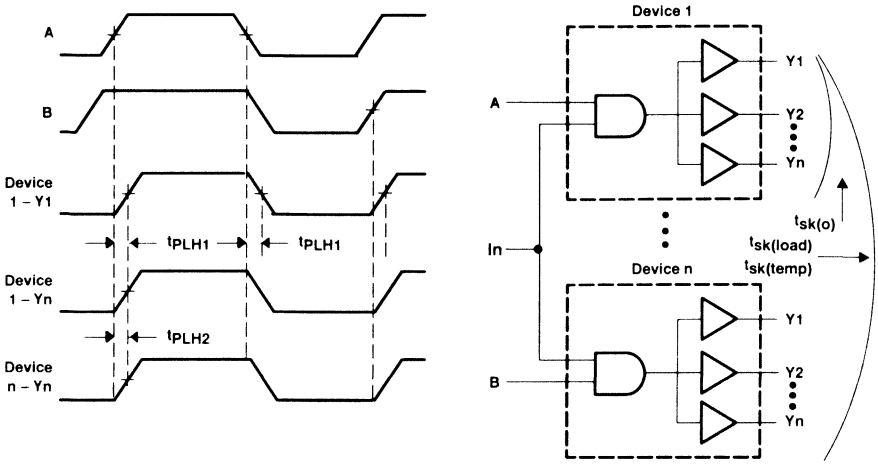
† t_r/t_f between V_O = 1 V/2 V
‡ t_r/t_f between 10% and 90% of output waveform
NOTE 4: Limits are specified but not tested.

extended output characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (see Note 4 and Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LOAD	SN54ABTE16245		SN74ABTE16245		UNIT
					MIN	MAX	MIN	MAX	
$t_{sk(temp)}$	A	B	V_{CC} = Constant, ΔT_A = 20°C			3		2.5	ns
	B	A		R_X = 56 Ω		4.5		4	
$t_{sk(load)}$	B	B	V_{CC} = Constant, Temperature = Constant	R_X = 13, 26, or 56 Ω		4.5		4	ns

NOTE 4: Limits are specified but not tested.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Pulse skew, $t_{sk(p)}$, is defined as the difference in propagation delay times t_{PLH1} and t_{PHL1} on the same terminal at identical operating conditions.

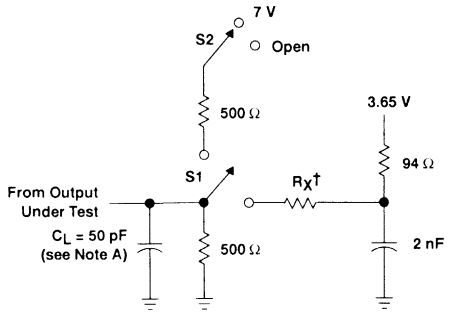
B. Output skew, $t_{sk(o)}$, is defined as the difference in propagation delay of the fastest and slowest paths on a single device that originate at either a single input or multiple simultaneously switched inputs, (e.g., $|t_{PLH1} - t_{PLH2}|$).

C. Temperature skew, $t_{sk(temp)}$, is the output skew of two devices, both having the same value of V_{CC} ± 1% and with package temperature differences of 20°C from each other.

D. Load skew, $t_{sk(load)}$, is measured with R_X in Figure 2 at 13 Ω for one unit and 56 Ω for the other unit.

Figure 1. Voltage Waveforms for Extended Characteristics

PARAMETER MEASUREMENT INFORMATION

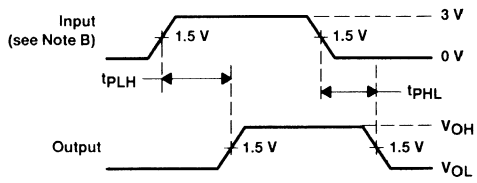


SWITCHING TABLE LOADS	S1	S2
t_{PLH}/t_{PHL} (A and B port)	Up	Open
t_{PLZ}/t_{PZL}	Up	7 V
t_{PHZ}/t_{PZH}	Up	Open

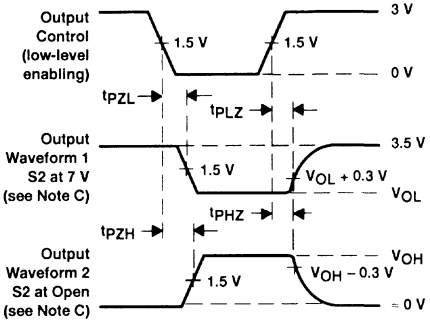
EXTENDED SWITCHING TABLE LOADS	S1	S2
$t_{PLH}/t_{PHL}/t_{sk}$ (A port)	Down	X
$t_{PLH}/t_{PHL}/t_{sk}$ (B port)	Up	Open
t_t (A port) (see Note E)	Down	X
t_t (B port) (see Note F)	Up	Open

† R_X = 13, 26, 56 Ω

LOAD CIRCUIT FOR OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



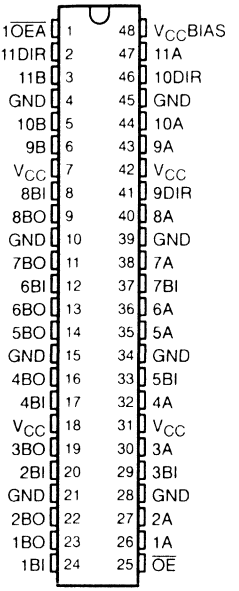
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.
E. t_t is measured at 1 V to 2 V.
F. t_t is measured at 10% to 90%.

Figure 2. Load Circuit and Voltage Waveforms

- **Supports the VME64 ETL Specification**
- **Reduced, TTL-Compatible, Input Threshold Range**
- **High-Drive Outputs (I_{OH} = –60 mA, I_{OL} = 90 mA) Support 25-Ω Incident-Wave Switching**
- **V_{CC}BIAS Pin Minimizes Signal Distortion During Live Insertion**
- **Internal Pullup Resistor on $\overline{OE}$ Keeps Outputs in High-Impedance State During Power Up or Power Down**
- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **25-Ω Series Dampening Resistor on B Port**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-Mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

SN54ABTE16246 . . . WD PACKAGE
SN74ABTE16246 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The 'ABTE16246 are 11-bit noninverting transceivers designed for synchronous two-way communication between buses. These devices consist of open-collector and 3-state outputs. They allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated. When $\overline{OE}$ is low, the device is active.

The B port has a 25-Ω series output resistor to reduce ringing. Active bus-hold inputs are also found on the B port to hold unused or floating inputs at a valid logic level.

The A port provides for the precharging of the outputs via V_{CC}BIAS, which establishes a voltage between 1.3 V and 1.7 V when V_{CC} is not connected.

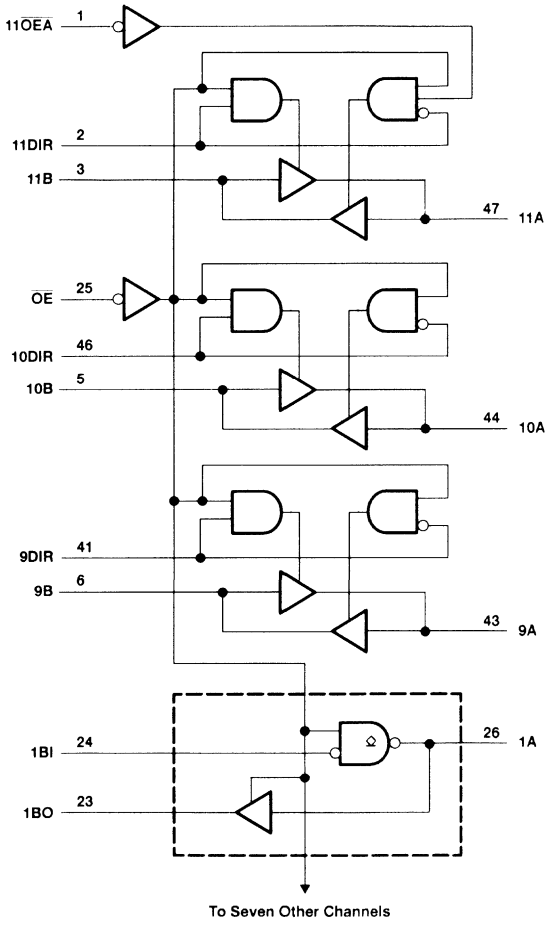
The SN74ABTE16246 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABTE16246 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABTE16246 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	A data to B bus
L	H	B data to A bus
H	X	Isolation

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) . . . . . −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O . . . . . −0.5 V to 5.5 V
Current into any output in the low state, I_O . . . . . 128 mA
Input clamp current, I_{IK} ($V_I < 0$) . . . . . −18 mA
Output clamp current, I_{OK} ($V_O < 0$) . . . . . −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DGG package . . . . . 0.85 W
DL package . . . . . 1.2 W
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 3)

			SN54ABTE16246			SN74ABTE16246			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	$\overline{OE}$	2			2			V
		Except $\overline{OE}$	1.6			1.6			
V_{IL}	Low-level input voltage	$\overline{OE}$			0.8			0.8	V
		Except $\overline{OE}$			1.4			1.4	
V_{OH}	High-level output voltage	1A–8A			5.5	0		5.5	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	B bus			−12			−12	mA
		9A–11A			−24			−64	
I_{OL}	Low-level output current	B bus			12			12	mA
		A bus			64			90	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10			10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 3: Unused or floating pins (input or A-bus I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			SN54ABTE16246			SN74ABTE16246			UNIT
					MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2			−1.2	V
V_{OH}	B port	V_{CC} = 5.5 V,	I_{OH} = − 100 µA				V_{CC}−0.2			V_{CC}−0.2	V
		V_{CC} = 4.5 V	I_{OH} = − 1 mA		2.4			2.4			
			I_{OH} = − 12 mA		2			2			
	9A–11A	V_{CC} = 5.5 V,	I_{OH} = − 1 mA				4.5			4.5	
		V_{CC} = 4.5 V	I_{OH} = − 32 mA		2.4			2.4			
			I_{OH} = − 64 mA					2			
I_{OH}	1A–8A	V_{CC} = 4.5 V,	V_{OH} = 5.5 V				20			20	µA
V_{OL}	B port	V_{CC} = 4.5 V	I_{OL} = 1 mA				0.4			0.4	V
			I_{OL} = 12 mA							0.8	
	A port	V_{CC} = 4.5 V	I_{OL} = 64 mA				0.55			0.55	
			I_{OL} = 90 mA							0.9	
$I_{I(hold)}$	B port	V_{CC} = 4.5 V	V_I = 0.8 V		100			100			µA
			V_I = 2 V		−100			−100			
		V_{CC} = 5.5 V,	V_I = 0 to 5.5 V				±500			±500	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = V_{CC} or GND				±1			±1	µA
	A or B ports						±20			±20	
I_{OZH}‡	9A–11A	V_{CC} = 5.5 V,	V_O = 2.7 V				10			10	µA
I_{OZL}‡	9A–11A	V_{CC} = 5.5 V,	V_O = 0.5 V				−10			−10	µA
I_O	A port	V_{CC} = 5.5 V,	V_O = 0		−50	−120	−180	−50		−180	µA
	B port				−25	−52	−90	−25		−90	
I_{off}		V_{CC} = 0, V_{CC}BIAS = 0	V_I or V_O ≤ 4.5 V,				±100			±100	µA
I_{CC}	A or B ports	V_{CC} = 5.5 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		28	36		28	36	mA
				Outputs low		38	48		38	48	
				Outputs disabled		20	32		20	32	
I_{CCD}	A or B ports	V_{CC} = 5 V,	C_L = 50 pF	$\overline{OE}$ high		0.02			0.02		mA/ MHz
				$\overline{OE}$ low		0.33			0.33		
C_i	Control inputs	V_I = 2.5 V or 0.5 V				2.5	4		2.5	4	pF
C_{io}	I/O ports	V_O = 2.5 V or 0.5 V				4.5	8		4.5	8	pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.

live-insertion specifications over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		SN54ABTE16246			SN74ABTE16246			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
I_{CC} (V_{CC}BIAS)		V_{CC} = 0 to 4.5 V, $I_{O(DC)}$ = 0	V_{CC}BIAS = 4.5 V to 5.5 V,		250	700		250	700	μA
		V_{CC} = 4.5 V to 5.5 V‡, $I_{O(DC)}$ = 0	V_{CC}BIAS = 4.5 V to 5.5 V,			20			20	
V_O	A port	V_{CC} = 0,	V_{CC}BIAS = 4.5 V to 5.5 V	1.1	1.5	1.9	1.1	1.5	1.9	V
		V_{CC} = 0,	V_{CC}BIAS = 4.75 V to 5.25 V	1.3	1.5	1.7	1.3	1.5	1.7	
I_O	A port	V_{CC} = 0, V_O = 0,	V_{CC}BIAS = 4.5 V	–20		–100	–20		–100	μA
		V_{CC} = 0, V_O = 3 V,	V_{CC}BIAS = 4.5 V	20		100	20		100	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ V_{CC} – 0.5 V < V_{CC}BIAS

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABTE16246		SN74ABTE16246		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1.5	3.1	4.2	1.5	5.4	1.5	5.2	ns
t_{PHL}			1.5	3.5	4.6	1.5	5.4	1.5	5.2	
t_{PLH}	9B–11B	9A–11A	1.5	3	3.8	1.5	4.7	1.5	4.5	ns
t_{PHL}			1.5	3.2	4	1.5	4.7	1.5	4.5	
t_{PLH}§	1B–8B	1A–8A	1.5	3.2	4	1.5	4.7	1.5	4.5	ns
t_{PLH}¶			7.5	8.9	9.7	7.5	10.6	7.5	10.3	ns
t_{PHL}			1.5	3.2	4	1.5	4.7	1.5	4.5	ns
t_{PZH}	$\overline{OE}$	9A–11A	2	4.3	5.3	2	6.4	2	6.2	ns
t_{PZL}		1A–11A	2	4.4	5.4	2	7	2	6.8	
t_{PZH}	$\overline{OE}$	B	2	4.3	6	2	7.3	2	7.1	ns
t_{PZL}			2	4.5	6.4	2	7.5	2	7.3	
t_{PHZ}	$\overline{OE}$	9A–11A	2	4.2	5.9	2	7	2	6.7	ns
t_{PLZ}		1A–11A	2	3.5	4.6	2	5.4	2	5.1	
t_{PHZ}	$\overline{OE}$	B	2.5	4.3	6.2	2.5	7.2	2.5	7	ns
t_{PLZ}			2	3.6	5	2	5.8	2	5.5	

§ Measurement point is V_{OL} + 0.3 V.
¶ Measurement point is V_{OL} + 1.5 V.

extended switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Note 4 and Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD	V_{CC} = 5 V, T_A = 25°C			SN54ABTE16246		SN74ABTE16246		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	9B–11B	9A–11A	R_X = 13 Ω	1.5	3.2	4	1.5	5	1.5	4.8	ns
t_{PHL}				1.5	3.8	4.7	1.5	5.8	1.5	5.6	
t_{PHL}	1B–8B	1A–8A	R_X = 13 Ω	1.5	3.3	4.2	1.5	5	1.5	4.8	ns
t_{PLH}	9B–11B	9A–11A	R_X = 26 Ω	1.5	3.1	4	1.5	4.8	1.5	4.6	ns
t_{PHL}				1.5	3.5	4.4	1.5	5.2	1.5	4.9	
t_{PHL}	1B–8B	1A–8A	R_X = 26 Ω	1.5	3.1	4	1.5	4.6	1.5	4.4	ns
t_{PLH}	9B–11B	1A–8A	R_X = 56 Ω	1.5	3	3.8	1.5	4.7	1.5	4.5	ns
t_{PHL}				1.5	3.3	4.2	1.5	5.1	1.5	4.7	
t_{PHL}	1B–8B	1A–8A	R_X = 56 Ω	1.5	3	4	1.5	4.6	1.5	4.4	ns
$t_{sk(p)}$	B	A	R_X = Open		0.1	0.6		2		2	ns
	A	B			0.4	0.8		2		2	
	B	A	R_X = 26 Ω		0.3	0.8		2		2	
$t_{sk(o)}$	B	A	R_X = Open		0.3	0.7		1.3		1.3	ns
	A	B			0.7	1.1		1.3		1.3	
	B	A	R_X = 26 Ω		0.5	1		1.3		1.3	
t_t†	B	A	R_X = 26 Ω	0.5	0.8	1.5	0.5	1.5	0.5	1.5	ns
t_t‡	A	B	Rise or fall time 10%–90%	3.5	5.5	7.3	3.5	8.1	3.5	7.9	ns

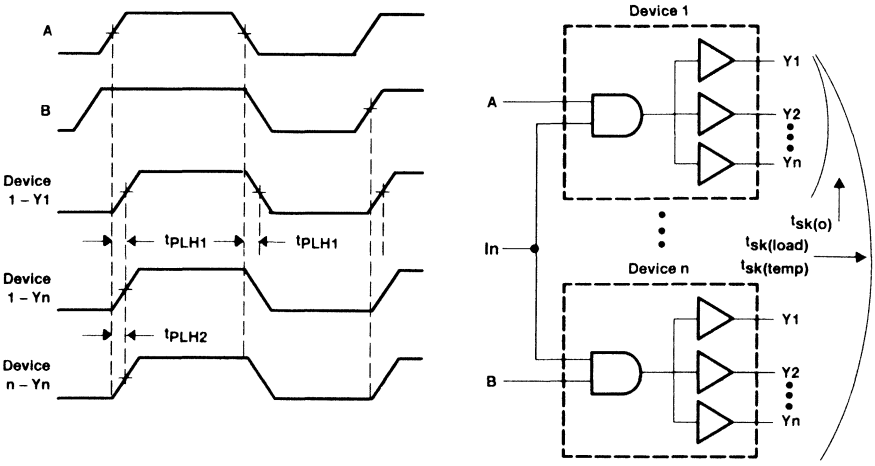
† t_r/t_f between V_O = 1 V/2 V.
‡ t_r/t_f between 10% and 90% of output waveform
NOTE 4: Limits are specified but not tested.

extended output characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (see Note 4 and Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LOAD	SN54ABTE16246		SN74ABTE16246		UNIT
					MIN	MAX	MIN	MAX	
$t_{sk(temp)}$	A	B	V_{CC} = Constant, ΔT_A = 20°C			3		2.5	ns
	B	A		R_X = 56 Ω		4.5		4	
$t_{sk(load)}$	B	A	V_{CC} = Constant, Temperature = Constant	R_X = 13, 26, or 56 Ω		4.5		4	ns

NOTE 4: Limits are specified but not tested.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Pulse skew, $t_{sk(p)}$, is defined as the difference in propagation delay times t_{PLH1} and t_{PHL1} on the same terminal at identical operating conditions.

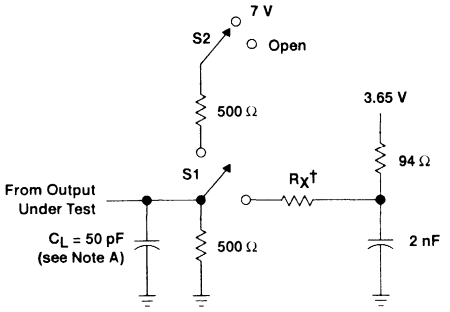
B. Output skew, $t_{sk(o)}$, is defined as the difference in propagation delay of the fastest and slowest paths on a single device that originate at either a single input or multiple simultaneously switched inputs, (e.g., $|t_{PLH1} - t_{PLH2}|$).

C. Temperature skew, $t_{sk(temp)}$, is the output skew of two devices, both having the same value of V_{CC} ± 1% and with package temperature differences of 20°C from each other.

D. Load skew, $t_{sk(load)}$, is measured with R_X in Figure 2 at 13 Ω for one unit and 56 Ω for the other unit.

Figure 1. Voltage Waveforms for Extended Characteristics

PARAMETER MEASUREMENT INFORMATION

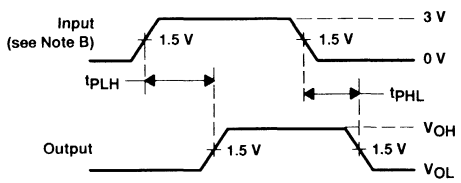


† R_X = 13, 26, 56 Ω

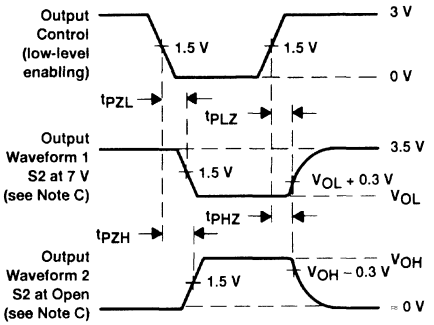
LOAD CIRCUIT FOR OUTPUTS

SWITCHING TABLE LOADS	S1	S2
t_{PLH}/t_{PHL} (9A – 11A and B port)	Up	Open
t_{PLH}/t_{PHL} (1A – 8A)	Up	7 V
t_{PLZ}/t_{PZL}	Up	7 V
t_{PHZ}/t_{PZH} (except 1A – 8A)	Up	Open

EXTENDED SWITCHING TABLE LOADS	S1	S2
$t_{PLH}/t_{PHL}/t_{sk}$ (A port)	Down	X
$t_{PLH}/t_{PHL}/t_{sk}$ (B port)	Up	Open
t_t (A port) (see Note E)	Down	X
t_t (B port) (see Note F)	Up	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.
E. t_t is measured at 1 V to 2 V.
F. t_t is measured at 10% to 90%.

Figure 2. Load Circuit and Voltage Waveforms

The demand for high-performance Backplane Transceiver Logic (BTL) and Futurebus+ (FB+) bus-interface devices continues to grow in telecommunications, networking, and mainframe applications. The BTL/FB+ standard uses a greatly reduced output swing and a tighter switching margin compared to the TTL standard.

The reduced-output BTL/FB+ transceivers from TI provide high drive and speed while minimizing skew and ground-bounce noise, and are compatible with IEEE 1194.1-1991 (BTL) and IEEE 896.2-1991 (FB+).

NEXT GENERATION FUTUREBUS+/BTL TRANSCEIVERS ALLOW SINGLE-SIDED SMT MANUFACTURING

INTRODUCTION

Futurebus+ (IEEE 896.2-1991) and BTL (IEEE 1194.1-1991) designs offer significant performance advantages over conventional TTL backplane implementations, but these advantages come with trade-offs. Switching noise in the form of ground bounce and EMI must be controlled, and proper termination schemes must be employed to ensure signal integrity in this high speed switching environment. Trade-offs for price in the form of total system solution vs. overall system performance are also of concern. This paper begins with the historical perspective on signal integrity issues addressed by the above cited IEEE bodies, and follows with new pioneering bus interface solutions to help reduce overall FB+ or BTL system costs and design complexities.

CURRENT GENERATION OF FB+/BTL TRANSCEIVERS

Pursuant to the above cited IEEE standards, a number of suppliers have developed BTL and/or Futurebus+ compliant transceiver solutions. These devices share the same reduced output swing and tight switching thresholds shown in Figure 1, and also include slew rate control circuitry as shown in Figure 2. The various devices differ considerably in wafer fab process technology, propagation delay performance, and other performance metrics (Table I).

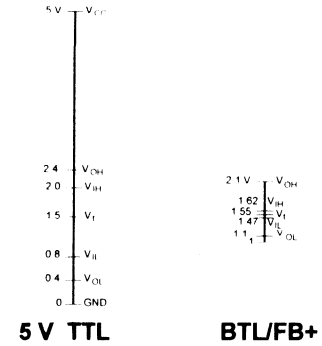


Fig. 1: Comparison of TTL and BTL switching standards

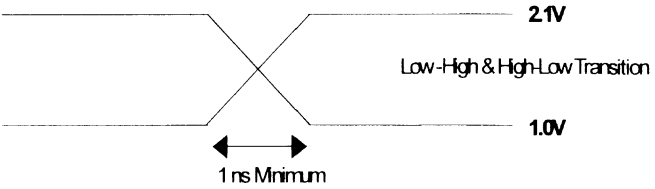


Fig 2: Illustration of Output Edge rate Control (OEC™)

Table I: BTL/Futurebus+ transceiver offering on available today

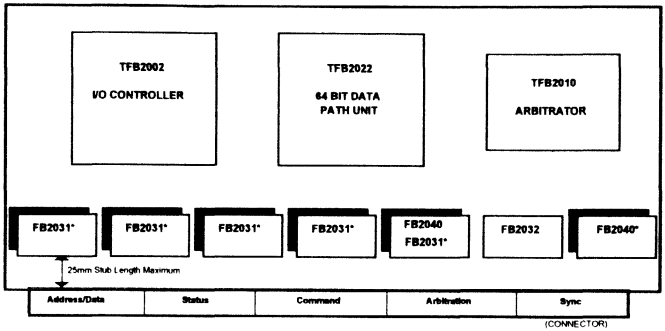
Transceiver	Technology	Bits/Pkg	Tpd
ALS056/057 ⊗	3μ Bipolar	4/8	20ns
DS3890 ⊗	2μ Bipolar	8*	15ns
DS3896/7 ⊗	1.5μ Bipolar	4/8	12ns
DS3893A ⊗	1.2μ Bipolar	4	7ns
FB2031/40	0.8μ BiCMOS	8/9	6ns

* Note: unidirectional driver only; not a true bi-directional transceiver
⊗ Note: not a TI product

The above table shows an evolutionary progression in bipolar wafer fab technology and hence faster propagation delay performance. Bipolar fab technologies are chosen for this class of device for their high drive capability, low switching noise, and relative ease of designing (relative to pure CMOS) the pseudo-analog circuitry required to meet the slew rate control requirement mentioned above. Bipolar circuits have the disadvantage of relatively high power dissipation. The heat generated by this high power dissipation coupled with the large switching currents coming from the bus termination place a thermal limitation on the number of bits that can be integrated into a single standard IC package (typically only 4 bits).

The newer class of BiCMOS transceivers employ a bipolar output structure to achieve the desired drive, noise, and slew rate control of the previous generation products. They also offer higher performance, much lower power dissipation, and take the next step towards higher integration (8 or 9 bits). However, even this level of density and performance is not totally sufficient for some emerging 128-bit applications. And at 9 bits, the devices are again up against the thermal capabilities of the packages: even with low power BiCMOS technology.

Futurebus+ (IEEE 896.2-1991) adds an additional constraint to board layout by mandating that all compliant cards have a maximum stub length of 25mm to reduce loading and minimize reflections. This is also a wise "rule of thumb" for non-Futurebus+ BTL designs. As data paths have increased in width from 32 to 64-bits (128-bits in the future), this stub length requirement has forced system designers to wrestle with the manufacturing problems of double- sided surface mounting of the transceivers on boards as large as 12 Standard Units (12SU). Even with the relatively dense packaging of today's fastest and most integrated transceivers, this can be a formidable design problem; adding significantly to the overall manufacturing cost of a board (Figure 3).



* Note: the "*" or second part type descriptor indicates that a second transceiver is mounted on the opposite side of the board

Fig 3: Uncached 64-bit FB+ layout with TI's controller chipset and today's most integrated transceivers

Another problem with the current generation of transceivers is the purchasing requirement for multiple transceiver types. Continuing with the above example, the common 64-bit uncached solution requires three different transceiver types for a complete distributed arbitration Futurebus+ implementation shown in Table II below.

Table II: Transceiver descriptions for 64-bit uncached FB+ board using FB20xx series transceivers

Device	Description	Qty/Board
FB2031	9-Bit Data/Address Xcver w/ Clk & Latch	9
FB2032*	Arbitration Contest Transceiver	1
FB2040	8-bit status/sync Xcver w/split TTL I/O	3
	TOTAL PART COUNT:	**13**

* Optional; for distributed arbitration only

These transceivers were designed quite differently from one another due to the specific functions they perform in the system (data/address, sync, arbitration, status, or command). Figure 4 highlights the functional differences between the FB2040 (status and sync transceiver) and the FB2031 (address/data transceiver). The main distinctions to note here are the "universal" storage modes (transparent, latched, or clocked) of the FB2031 and the separate or "split" TTL I/O pins of the FB2040. And as noted above, until recently, efforts to develop any sort of true universal FB+/BTL transceiver have not been practical due to the absence of a viable high-power fine pitch package beyond 56 pins in the industry.

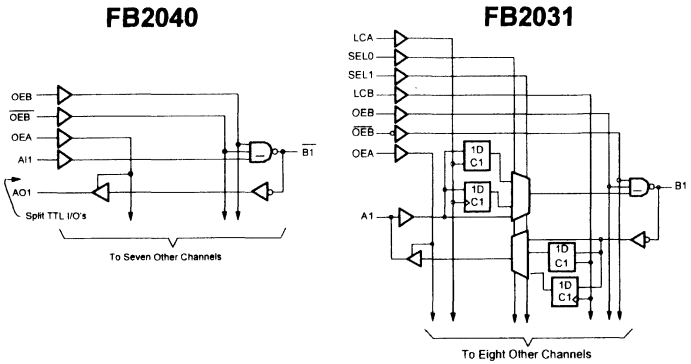


Fig 4: Functional differences between FB2040 control transceiver and FB2031 address/data transceiver

A NEW GENERATION OF FB+/BTL TRANSCEIVERS

As a response to the market need for single-sided surface mounting and simplified transceiver architectures, TI has developed both a high-power package and a series of 18-channel FB+/BTL Universal Bus Transceivers (UBT™). These new devices, designated as FB16xxx series, are packaged in a high-power version of the EIAJ standard 100-pin TQFP package (0.5mm lead pitch). A package cross section is shown in figure 5 which reveals a metal heat sink that facilitates the excellent thermal performance of the package.

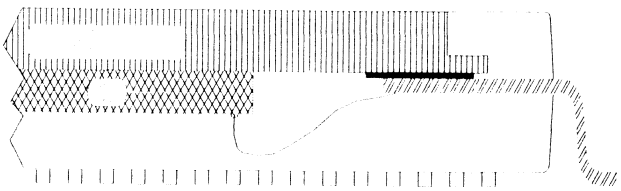


Fig 5: Cross section of thermally enhanced EIAJ 100 TQFP

The FB16xxx series devices are designed with both the universal data storage capabilities of the FB2031 address/data transceiver and the separate TTL I/O of the FB2040 control transceiver, and can be configured as two independent 9-channel or one coherent 18-channel transceiver (figure 6).

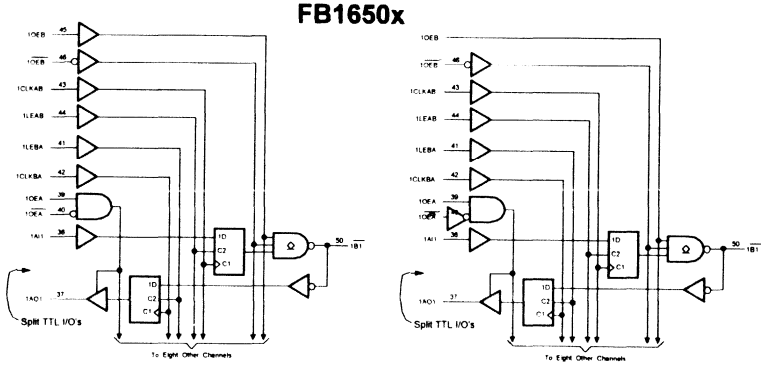
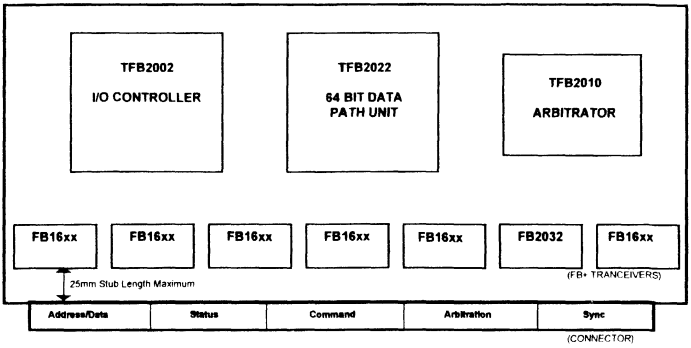


Fig 6: Functional circuit diagram of FB1650x

This flexible design approach eliminates the need for double-sided surface mounting--along with all of the associated manufacturing costs--and still meets the IEEE 896.2-1991 25mm maximum stub length requirements as shown in Figure 7.



* Note: no double sided SMT requirement

Fig 7: Uncached 64-bit FB+ layout with TI chipset and FB16xxx transceivers

In addition, the 18 channel architecture lends itself naturally to reduced pin to pin signal skew, and advanced BiCMOS circuit design techniques have been employed to improve propagation delay performance over the previous generation of BiCMOS transceivers. Table III offers a transceiver component count comparison for the same 64-bit uncached Futurebus+ example considered previously.

Table III: Component count comparison for 64-bit uncached FB+ board using FB16xxx series transceivers

Device	Description	Qty/Board
FB16xxx	18-bit TTL/BTL UBT w/split TTL I/O	6
FB2032*	Arbitration Contest Transceiver	1
	TOTAL PART COUNT:	**7**

* Optional; for distributed arbitration only

This represents nearly a 50% reduction in component count and a cost savings of ca. 14% on the transceivers alone. Significant savings (tens of dollars per board) on manufacturing costs are also realized by moving to single-sided SMT manufacturing. Other members of the FB16xxx family include system clock distribution features that lend themselves to more specific end system applications such as ATM hubs and routers (Table IV):

Table IV: Transceiver descriptions for other members of FB16xxx series

Device	Description
FB1650x	18-bit TTL/BTL UBT w/split TTL I/O
FB1651x	17-Channel UBT w/ Separate Buffered and Delayed Clk Bit
FB1652x	17-Channel UBT w/ Separate Buffered Clk Bit (No Delay Line)

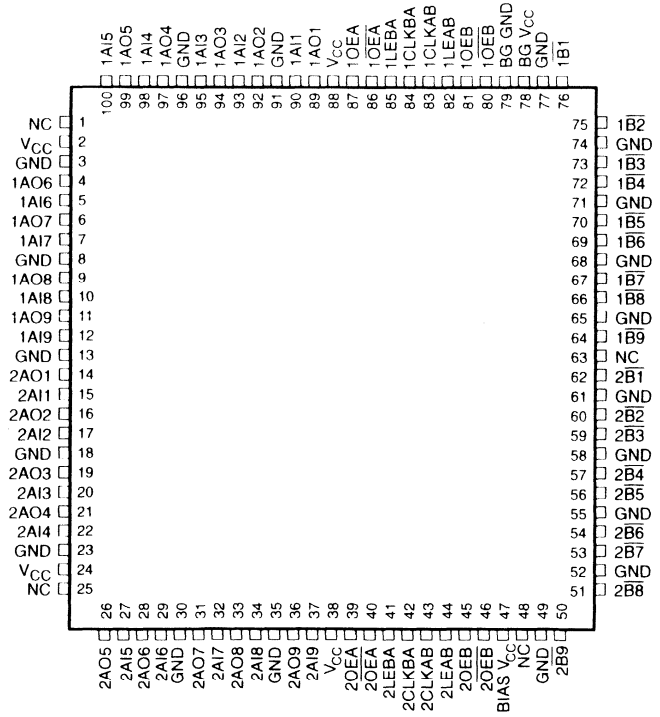
CONCLUSION

The high speed data communication requirements of today's fastest board level computers and telecommunications and network switching equipments can be met with Futurebus+ and BTL compatible transceivers and switching levels. Stub length constraints and ever increasing data path widths have made it difficult to control signal integrity and manufacturing and procurement costs in these high performance systems. The next generation of 18-channel FB+/BTL Universal Bus Transceivers meets this market need by facilitating low cost single-sided surface mount manufacturing, and single-device type procurement, characterization, qualification, and specification.

SCBS178D – AUGUST 1992 – REVISED JULY 1995

- **Compatible With IEEE 1194.1-1991 (BTL) Standard**
- **TTL A Port, Backplane Transceiver Logic $\overline{B}$ Port**
- **Open-Collector $\overline{B}$-Port Outputs Sink 100 mA**
- **Isolated Logic-Ground and Bus-Ground Pins Reduce Noise**
- **BIAS V_{CC} Minimizes Signal Distortion During Live Insertion/Withdrawal**
- **$\overline{B}$-Port Biasing Network Preconditions the Connector and PC Trace to the Backplane Transceiver Logic High-Level Voltage**
- **TTL Input Structures Incorporate Active Clamping to Aid in Line Termination**
- **Package Options Include High-Power Shrink Quad Flat (PCA) Package With 0.5-mm Pin Pitch and Ceramic Quad Flat (HQA) Package**

SN54FB1650 . . . HQA PACKAGE
SN74FB1650 . . . PCA PACKAGE
(TOP VIEW)



NC – No internal connection

TEXAS INSTRUMENTS

description

The 'FB1650 contain two 9-bit transceivers designed to translate signals between TTL and backplane transceiver logic (BTL) environments. They are specifically designed to be compatible with the IEEE 1194.1-1 (BTL) standard.

The $\overline{B}$ port operates at BTL-signal levels. The open-collector $\overline{B}$ ports are specified to sink 100 mA. Two output enables (OEB and $\overline{OEB}$) are provided for the $\overline{B}$ outputs. When OEB is low, $\overline{OEB}$ is high, or V_{CC} is typically less than 2.5 V, the $\overline{B}$ port is turned off.

The A port operates at TTL-signal levels. The A outputs reflect the inverse of the data at the $\overline{B}$ port when the A-port output enable (OEA) is high. When OEA is low or when V_{CC} is typically less than 2.5 V, the A outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating TTL inputs at a valid logic state.

BIAS V_{CC} establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when V_{CC} is not connected.

BG V_{CC} and BG GND are the supply inputs for the bias generator.

The SN54FB1650 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74FB1650 is characterized for operation from 0°C to 70°C.

Function Tables

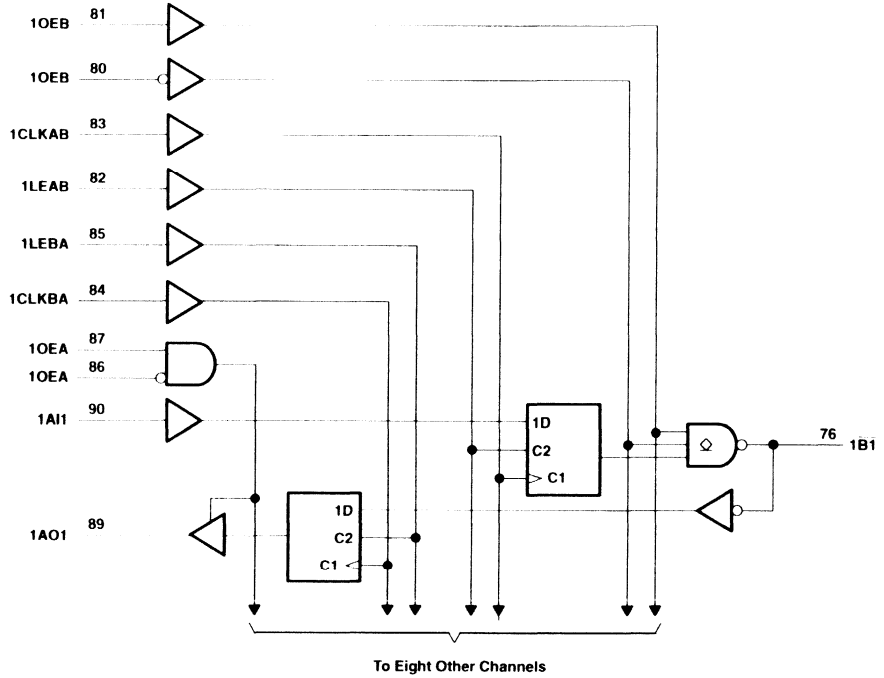
TRANSCEIVER

INPUTS				FUNCTION
OEA	OEA	OEB	OEB	
X	X	H	L	A data to B bus
L	H	X	X	B data to A bus
L	H	H	L	A data to B bus, B data to A bus
X	X	L	X	B-bus isolation
X	X	X	H	
H	X	X	X	A-bus isolation
X	L	X	X	

STORAGE MODE

INPUTS		FUNCTION
LE	CLK	
H	X	Transparent
L	↑	Store data
L	L	Storage

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}, BIAS V_{CC}, BG V_{CC} . . . . . −0.5 V to 7 V
Input voltage range, V_I: except $\overline{B}$ port . . . . . −1.2 V to 7 V
$\overline{B}$ port . . . . . −1.2 V to 3.5 V
Voltage range applied to any $\overline{B}$ output in the disabled or power-off state, V_O . . . . . −0.5 V to 5.5 V
Voltage range applied to any output in the high state, V_O . . . . . −0.5 V to V_{CC}
Input current range (except $\overline{B}$ port) . . . . . −40 mA to 5 mA
Current applied to any single output in the low state, I_O: A port . . . . . 48 mA
$\overline{B}$ port . . . . . 200 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 1): PCA package . . . . . 1.8 W
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 75 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 2)

			SN54FB1650			SN74FB1650			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}, BG V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
BIAS V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	B port	1.62		2.3	1.62		2.3	V
		Except $\overline{B}$ port	2			2			
V_{IL}	Low-level input voltage	B port	0.75		1.47	0.75		1.47	V
		Except $\overline{B}$ port			0.8			0.8	
I_{IK}	Input clamp current				–18			–18	mA
I_{OH}	High-level output current	A port			–3			–3	mA
I_{OL}	Low-level output current	A port			24			24	mA
		$\overline{B}$ port			100			100	
T_A	Operating free-air temperature		–55		125	0		70	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		SN54FB1650			SN74FB1650			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$\overline{B}$ port	V_{CC} = 4.5 V	I_I = –18 mA			–1.2			–1.2	V
	Except $\overline{B}$ port		I_I = –40 mA			–0.5			–0.5	
V_{OH}	AO port	V_{CC} = 4.5 V	I_{OH} = –1 mA							V
			I_{OH} = –3 mA	2.5	3.3		2.5	3.3		
V_{OL}	AO port	V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.35	0.5		0.35	0.5	V
	$\overline{B}$ port	V_{CC} = 4.5 V	I_{OL} = 80 mA	0.75		1.1	0.75		1.1	
			I_{OL} = 100 mA			1.15			1.15	
I_I	Except $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 5.5 V			50			50	µA
I_{IH}‡	Except $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 2.7 V			50			50	µA
I_{IL}‡	Except $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 0.5 V			–50			–50	µA
	B port	V_{CC} = 5.5 V,	V_I = 0.75 V			–100			–100	
I_{OZH}	AO port	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	µA
I_{OZL}	AO port	V_{CC} = 5.5 V,	V_O = 0.5 V			–50			–50	µA
I_{OZPU}	AO port	V_{CC} = 0 to 2.1 V,	V_O = 0.5 to 2.7 V			50			50	µA
I_{OZPD}	AO port	V_{CC} = 2.1 V to 0,	V_O = 0.5 to 2.7 V			–50			–50	µA
I_{OH}	$\overline{B}$ port	V_{CC} = 0 to 5.5 V,	V_O = 2.1 V			100			100	µA
I_{OS}§	A port	V_{CC} = 5.5 V,	V_O = 0	–30		–150	–30		–150	mA
I_{CC}	A port to $\overline{B}$ port	V_{CC} = 5.5 V,	I_O = 0			100			100	mA
	$\overline{B}$ port to A port					120			120	
C_i	AI port	V_I = V_{CC} or GND			5.5			5.5		pF
	Control pins				5.5			5.5		
C_o	AO ports	V_O = V_{CC} or GND			5.5			5.5		pF
C_{io}¶	$\overline{B}$ port per P1194.0	V_{CC} = 0 to 5.5 V				5.5			5.5	pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
¶ Parameter is based on characterization but is not tested.

live-insertion specifications over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		SN54FB1650		SN74FB1650		UNIT
				MIN	MAX	MIN	MAX	
I_{CC} (BIAS V_{CC})		V_{CC} = 0 to 4.5 V	V_B = 0 to 2 V, V_I (BIAS V_{CC}) = 4.5 V to 5.5 V		50		450	µA
		V_{CC} = 4.5 V to 5.5 V			10		10	
V_O	B port	V_{CC} = 0,	V_I (BIAS V_{CC}) = 4.5 V to 5.5 V	1.62	2.1	1.62	2.1	V
I_O	B port	V_{CC} = 0, V_B = 1 V,	V_I (BIAS V_{CC}) = 4.5 V to 5.5 V			−1		µA
		V_{CC} = 0 to 5.5 V,	OEB = 0 to 0.8 V		100		100	
		V_{CC} = 0 to 2.2 V,	OEB = 0 to 5 V		100		100	

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

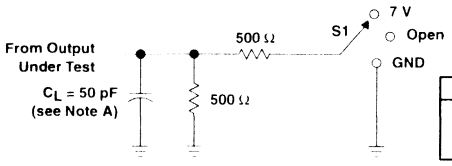
			V_{CC} = 5 V, T_A = 25°C		SN54FB1650		SN74FB1650		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	150	0	150	0	150	MHz
t_w	Pulse duration, CLK or LE		3.3		3.3		3.3		ns
t_{su}	Setup time	Data before LE	4.8		5.5		4.8		ns
		Data before CLK↑	4.9		5		4.9		
t_h	Hold time	Data after LE	1.8		2.8		1.8		ns
		Data after CLK↑	1.1		1.1		1.1		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

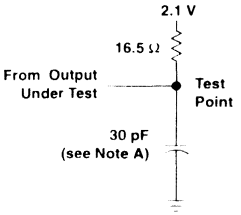
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54FB1650		SN74FB1650		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
f_{max}			150			150		150		MHz
t_{PLH}	AI	B	1.8	3.7	5.3	1.8	6.6	1.8	6.2	ns
t_{PHL}			2.9	4.4	6	2.9	7.3	2.9	7.2	
t_{PLH}	LEAB	B	2.7	4.2	5.8	2.7	6.9	2.7	6.4	ns
t_{PHL}			3.5	5	6.5	3.5	7.5	3.5	7.3	
t_{PLH}	CLKAB	$\overline{B}$	2.3	3.9	5.5	2.3	6.5	2.3	6	ns
t_{PHL}			2.9	4.5	6.1	2.9	6.8	2.9	6.7	
t_{PLH}	B	AO	3.5	5.9	7.9	3.5	9.7	3.5	8.6	ns
t_{PHL}			2.2	3.7	5.3	2.2	6	2.2	5.7	
t_{PLH}	LEBA	AO	1.8	3.2	4.6	1.8	5.4	1.8	5.1	ns
t_{PHL}			1.7	3	4.4	1.7	5.1	1.7	4.7	
t_{PLH}	CLKBA	AO	1.8	3.1	4.6	1.8	5.3	1.8	5.1	ns
t_{PHL}			1.7	3.1	4.6	1.7	5.3	1.7	4.9	
t_{PLH}	OEB	$\overline{B}$	2.7	4.6	6.4	2.7	7.4	2.7	6.7	ns
t_{PHL}			2.9	4.1	5.9	2.9	6.8	2.9	6.6	
t_{PLH}	OEB	B	2.6	4.3	6.2	2.6	7.2	2.6	6.6	ns
t_{PHL}			3.4	4.6	6.4	3.4	7.2	3.4	7	
t_{PZH}	OEA	AO	1.4	2.9	4.4	1.4	5.3	1.4	4.9	ns
t_{PZL}			1.4	2.6	4	1.4	4.9	1.4	4.6	
t_{PHZ}	OEA	AO	1.7	3.4	5.1	1.7	5.9	1.7	5.8	ns
t_{PLZ}			2.2	3.6	5	2.2	5.8	2.2	5.5	
t_{PZH}	OEA	AO	1.7	3.3	4.7	1.7	5.9	1.7	5.5	ns
t_{PZL}			1.7	3.1	4.4	1.7	5.4	1.7	5.1	
t_{PHZ}	$\overline{OEA}$	AO	1.5	2.9	4.5	1.5	5.2	1.5	5.1	ns
t_{PLZ}			2	3.1	4.6	2	5	2	4.8	
$t_{sk(p)}$‡ Skew for any single channel $\lvert t_{PHL} - t_{PLH} \rvert$		AI to $\overline{B}$ or $\overline{B}$ to AO		0.5						ns
$t_{sk(o)}$‡ Skew between drivers in the same package		AI to $\overline{B}$ or $\overline{B}$ to AO		1						ns
t_t	Transition time, $\overline{B}$ outputs (1.3 V to 1.8 V)		0.9	1.7	3.1	0.3	6.8	0.5	4.6	ns
	Transition time, AO outputs (10% to 90%)		0.5	2	3.6	0.3	4.3	0.4	4.2	
t_{PR}	$\overline{B}$-port input pulse rejection		1			1		1		ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Skew values are applicable for through mode only.

PARAMETER MEASUREMENT INFORMATION

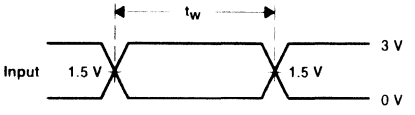


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

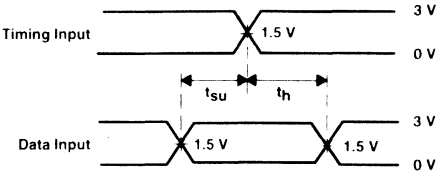


LOAD CIRCUIT FOR A OUTPUTS

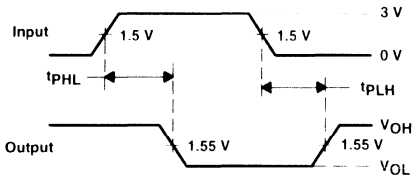
LOAD CIRCUIT FOR B OUTPUTS



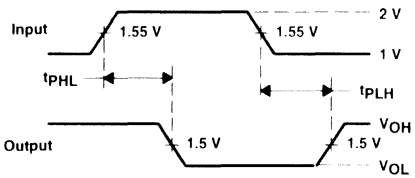
VOLTAGE WAVEFORMS
PULSE DURATION



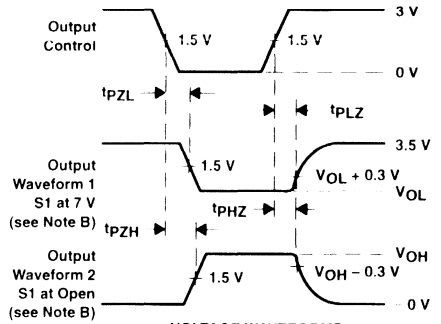
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (A to B)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (B to A)



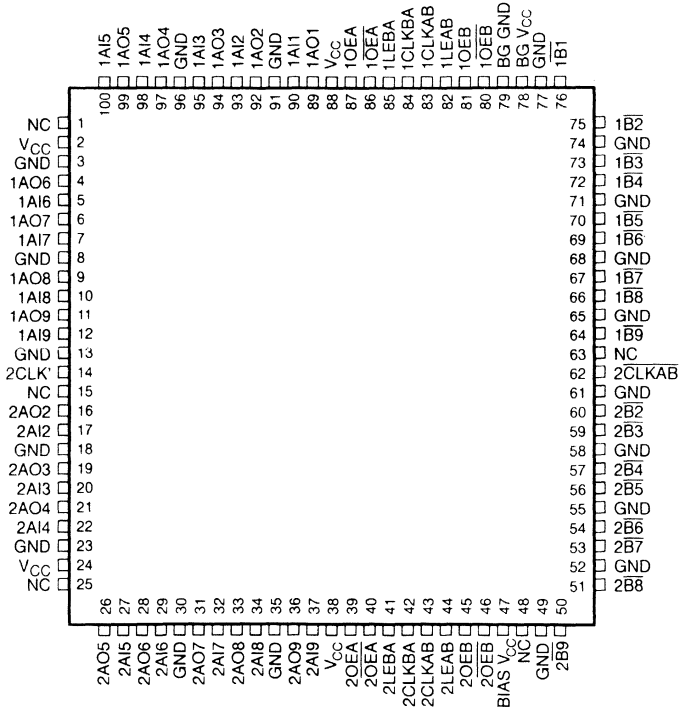
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES (A port)

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: TTL inputs – PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns. BTL inputs – PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

- Compatible With IEEE 1194.1-1991 (BTL) Standard
- TTL A Port, Backplane Transceiver Logic $\overline{B}$ Port
- Open-Collector $\overline{B}$-Port Outputs Sink 100 mA
- Isolated Logic-Ground and Bus-Ground Pins Reduce Noise
- $\overline{B}$-Port Biasing Network Preconditions the Connector and PC Trace to the Backplane Transceiver Logic High-Level Voltage
- TTL Input Structures Incorporate Active Clamping to Aid in Line Termination
- Package Options Include High-Power Shrink Quad Flat (PCA) Package With 0.5-mm Pin Pitch and Ceramic Quad Flat (HQA) Package

SN54FB1651 . . . HQA PACKAGE
SN74FB1651 . . . PCA PACKAGE
(TOP VIEW)



NC – No internal connection

TEXAS INSTRUMENTS

description

The 'FB1651 contain an 8-bit and a 9-bit transceiver with a buffered clock. The clock and the transceivers are designed to translate signals between TTL and backplane transceiver logic (BTL) environments. They are specifically designed to be compatible with the IEEE 1194.1-1 (BTL) standard.

The $\overline{B}$ port operates at BTL-signal levels. The open-collector $\overline{B}$ ports are specified to sink 100 mA. Two output enables (OEB and $\overline{OEB}$) are provided for the $\overline{B}$ outputs. When OEB is low, $\overline{OEB}$ is high, or V_{CC} is typically less than 2.5 V, the $\overline{B}$ port is turned off.

The A port operates at TTL-signal levels. The A outputs reflect the inverse of the data at the $\overline{B}$ port when the A-port output enable (OEA) is high. When OEA is low or when V_{CC} is typically less than 2.5 V, the A outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating TTL inputs at a valid logic state.

BIAS V_{CC} establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when V_{CC} is not connected.

BG V_{CC} and BG GND are the supply inputs for the bias generator.

The SN54FB1651 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74FB1651 is characterized for operation from –40°C to 85°C.

Function Tables

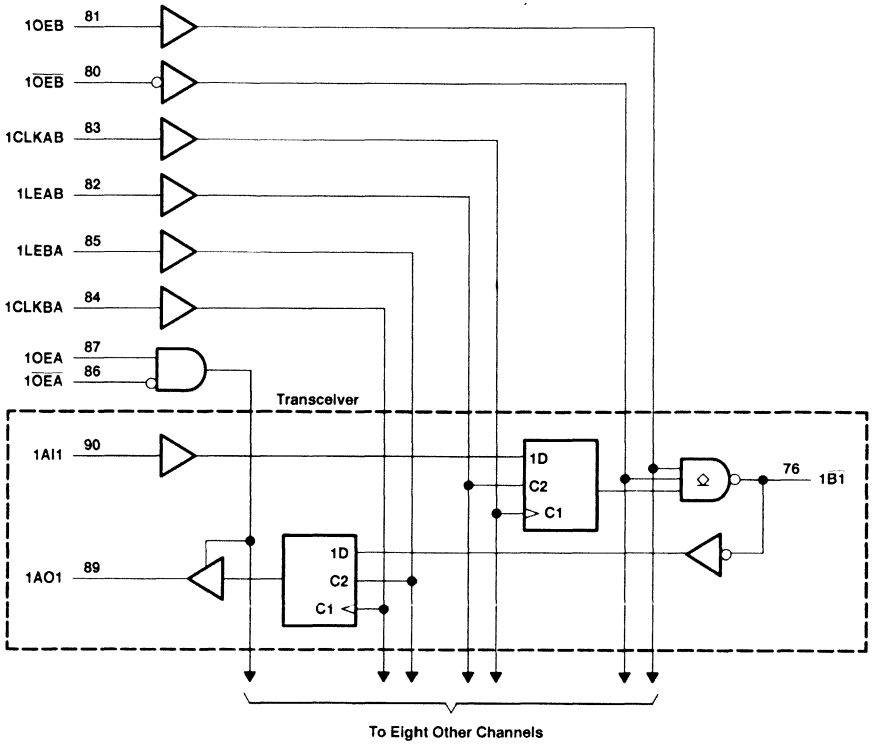
TRANSCEIVER

INPUTS				FUNCTION
$\overline{OEA}$	OEA	OEB	$\overline{OEB}$	
X	X	H	L	$\overline{A}$ data to B bus
L	H	X	X	$\overline{B}$ data to A bus
L	H	H	L	$\overline{A}$ data to B bus, $\overline{B}$ data to A bus
X	X	L	X	B-bus isolation
X	X	X	H	
H	X	X	X	A-bus isolation
X	L	X	X	

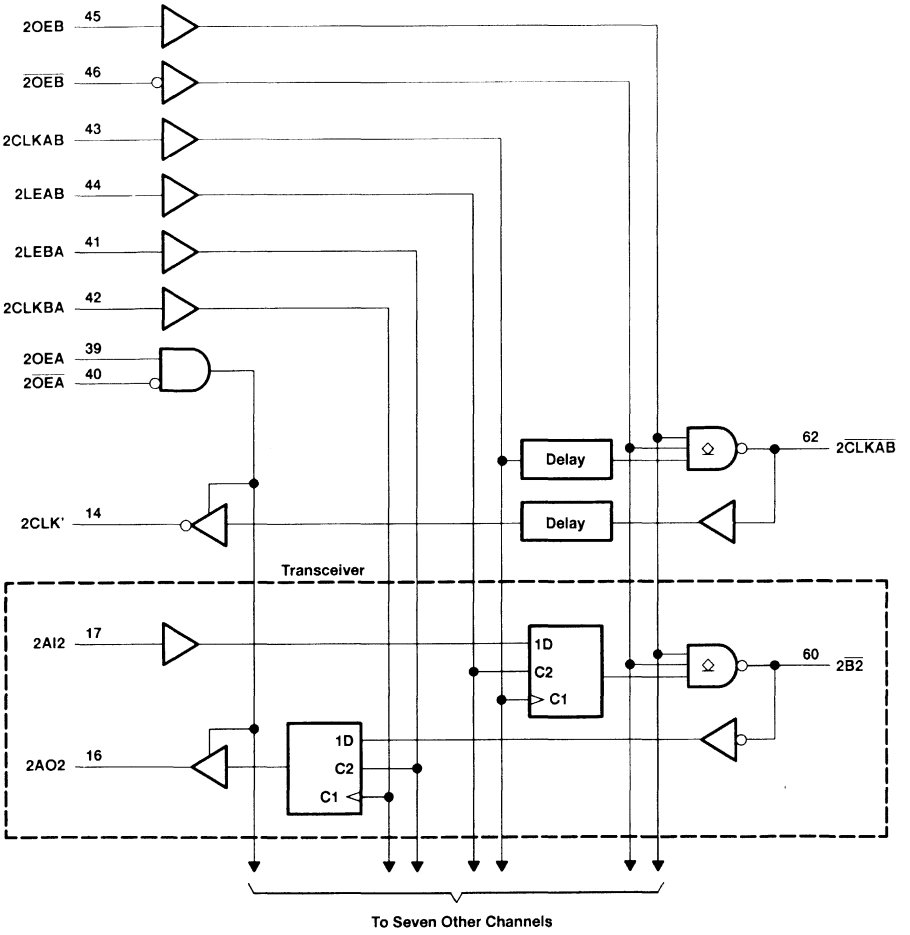
STORAGE MODE

INPUTS		FUNCTION
LE	CLK	
H	X	Transparent
L	↑	Store data
L	L	Storage

functional block diagram



functional block diagram (continued)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}, BIAS V_{CC}, BG V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I: except $\overline{B}$ port ..... −1.2 V to 7 V
$\overline{B}$ port ..... −1.2 V to 3.5 V
Input current range (except $\overline{B}$ port) ..... −40 mA to 5 mA
Voltage range applied to any $\overline{B}$ output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage range applied to any output in the high state ..... −0.5 V to V_{CC}
Current applied to any single output in the low state: A port ..... 48 mA
$\overline{B}$ port ..... 200 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 1): PCA package ..... 1.8 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 75 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 2)

			SN54FB1651			SN74FB1651			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}, BG V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
BIAS V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	$\overline{B}$ port	1.62		2.3	1.62		2.3	V
		Except $\overline{B}$ port	2			2			
V_{IL}	Low-level input voltage	$\overline{B}$ port	0.75		1.47	0.75		1.47	V
		Except $\overline{B}$ port			0.8			0.8	
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	High-level output current	A port			−3			−3	mA
I_{OL}	Low-level output current	A port			24			24	mA
		$\overline{B}$ port			100			100	
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		SN54FB1651			SN74FB1651			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	AO port	V_{CC} = 4.5 V	I_{OH} = −1 mA							V
			I_{OH} = −3 mA	2.5	3.3		2.5	3.3		
V_{OL}	AO port	V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.35	0.5		0.35	0.5	V
	$\overline{B}$ port	V_{CC} = 4.5 V	I_{OL} = 80 mA	0.75		1.1	0.75		1.1	
			I_{OL} = 100 mA			1.15			1.15	
I_I	Except $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 5.5 V			50			50	µA
I_{IH}‡	Except $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 2.7 V			50			50	µA
I_{IL}‡	Except $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 0.5 V			−50			−50	µA
	$\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 0.75 V			−100			−100	
I_{OZH}	AO port	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	µA
I_{OZL}	AO port	V_{CC} = 5.5 V,	V_O = 0.5 V			−50			−50	µA
I_{OZPU}	AO port	V_{CC} = 0 to 2.1 V,	V_O = 0.5 to 2.7 V			50			50	µA
I_{OZPD}	AO port	V_{CC} = 2.1 V to 0,	V_O = 0.5 to 2.7 V			−50			−50	µA
I_{OH}	$\overline{B}$ port	V_{CC} = 0 to 5.5 V,	V_O = 2.1 V			100			100	µA
I_{OS}§	A port	V_{CC} = 5.5 V,	V_O = 0	−30		−150	−30		−150	mA
I_{CC}	A port to $\overline{B}$ port	V_{CC} = 5.5 V,	I_O = 0			100			100	mA
	$\overline{B}$ port to A port					120			120	
C_i	AI port	V_I = V_{CC} or GND			5.5			5.5		pF
	Control pins				5.5			5.5		
C_o	AO ports	V_O = V_{CC} or GND			5.5			5.5		pF
C_{io}	$\overline{B}$ port per P1194.0	V_{CC} = 0 to 5.5 V				5.5			5.5	pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

live-insertion specifications over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS	TEST CONDITIONS	SN54FB1651		SN74FB1651		UNIT
				MIN	MAX	MIN	MAX	
I_{CC} (BIAS V_{CC})		V_{CC} = 0 to 4.5 V	V_B = 0 to 2 V, V_I (BIAS V_{CC}) = 4.5 V to 5.5 V		450		450	µA
		V_{CC} = 4.5 V to 5.5 V			10		10	
V_O	$\overline{B}$ port	V_{CC} = 0,	V_I (BIAS V_{CC}) = 4.5 V to 5.5 V	1.62	2.1	1.62	2.1	V
I_O	$\overline{B}$ port	V_{CC} = 0, V_B = 1 V,	V_I (BIAS V_{CC}) = 4.5 V to 5.5 V			−1		µA
		V_{CC} = 0 to 5.5 V,	OEB = 0 to 0.8 V		100		100	
		V_{CC} = 0 to 2.2 V,	OEB = 0 to 5 V		100		100	

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

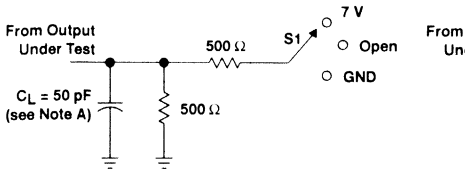
			V_{CC} = 5 V, T_A = 25°C		SN54FB1651		SN74FB1651		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	150		150		150	MHz
t_w	Pulse duration	CLK or LE	3.3		3.3		3.3		ns
t_{su}	Setup time	Data before LE	4.8		5.5		4.8		ns
		Data before CLK↑	4.9		5		4.9		
t_h	Hold time	Data after LE	1.8		1.8		1.8		ns
		Data after CLK↑	1.1		1.1		1.1		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

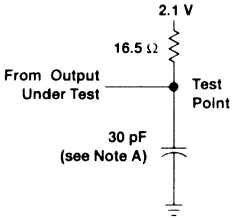
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54FB1651		SN74FB1651		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
f_{max}			150			150		150		MHz
t_{PLH}	AI	$\overline{B}$	1.8	3.7	5.3	1.8	6.6	1.8	6.2	ns
t_{PHL}			2.9	4.4	6	2.9	7.3	2.9	7.2	
t_{PLH}	LEAB	$\overline{B}$	2.7	4.2	5.8	2.7	6.9	2.7	6.4	ns
t_{PHL}			3.5	5	6.5	3.5	7.5	3.5	7.3	
t_{PLH}	CLKAB	$\overline{B}$	2.3	3.9	5.5	2.3	6.5	2.3	6	ns
t_{PHL}			2.9	4.5	6.1	2.9	6.8	2.9	6.7	
t_{PLH}	2CLKAB	$\overline{2CLKAB}$	4.6	6.9	8.8	4.6	10.7	4.6	9.9	ns
t_{PHL}			4.9	6.5	8.1	4.9	9.2	4.9	8.8	
t_{PLH}	$\overline{B}$	AO	3.5	5.9	7.9	3.5	9.7	3.5	8.6	ns
t_{PHL}			2.2	3.7	5.3	2.2	6	2.2	5.7	
t_{PLH}	LEBA	AO	1.8	3.2	4.6	1.8	5.4	1.8	5.1	ns
t_{PHL}			1.7	3	4.4	1.7	5.1	1.7	4.7	
t_{PLH}	CLKBA	AO	1.8	3.1	4.6	1.8	5.3	1.8	5.1	ns
t_{PHL}			1.7	3.1	4.6	1.7	5.3	1.7	4.9	
t_{PLH}	2CLKBA	2CLK'	6.4	9.7	11.8	6.4	15	6.4	13.4	ns
t_{PHL}			4.1	6.9	8.9	4.1	11.2	4.1	10.3	
t_{PLH}	OEB	$\overline{B}$	2.7	4.6	6.4	2.7	7.4	2.7	6.7	ns
t_{PHL}			2.9	4.1	5.9	2.9	6.8	2.9	6.6	
t_{PLH}	$\overline{OEB}$	$\overline{B}$	2.6	4.3	6.2	2.6	7.2	2.6	6.6	ns
t_{PHL}			3.4	4.6	6.4	3.4	7.2	3.4	7	
t_{PZH}	OEA	AO	1.4	2.9	4.4	1.4	5.3	1.4	4.9	ns
t_{PZL}			1.4	2.6	4	1.4	4.9	1.4	4.6	
t_{PHZ}	OEA	AO	1.7	3.4	5.1	1.7	5.9	1.7	5.8	ns
t_{PLZ}			2.2	3.6	5	2.2	5.8	2.2	5.5	
t_{PZH}	$\overline{OEA}$	AO	1.7	3.3	4.7	1.7	5.9	1.7	5.5	ns
t_{PZL}			1.7	3.1	4.4	1.7	5.4	1.7	5.1	
t_{PHZ}	$\overline{OEA}$	AO	1.5	2.9	4.5	1.5	5.2	1.5	5.1	ns
t_{PLZ}			2	3.1	4.6	2	5	2	4.8	
$t_{sk(p)}$‡ Skew for any single channel | $t_{PHL} - t_{PLH}$ |		AI to $\overline{B}$ or $\overline{B}$ to AO		0.5						ns
$t_{sk(o)}$‡ Skew between drivers in the same package		AI to $\overline{B}$ or $\overline{B}$ to AO		1						ns
t_t	Transition time, $\overline{B}$ outputs (1.3 V to 1.8 V)		0.9	1.7	3.1	0.3	6.8	0.5	4.6	ns
	Transition time, AO outputs (10% to 90%)		0.5	2	3.6	0.3	4.3	0.4	4.2	
t_{PR}	$\overline{B}$-port input pulse rejection		1			1		1		ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Skew values are applicable for through mode only.

PARAMETER MEASUREMENT INFORMATION

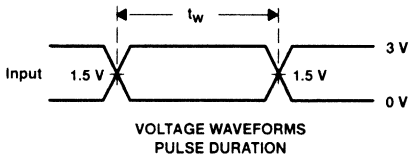


LOAD CIRCUIT FOR A OUTPUTS

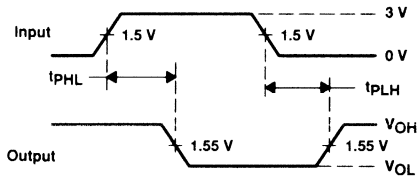


LOAD CIRCUIT FOR B OUTPUTS

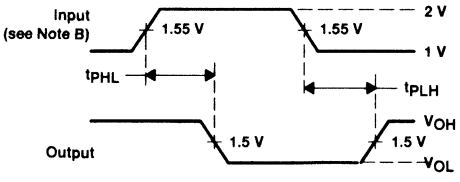
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	GND



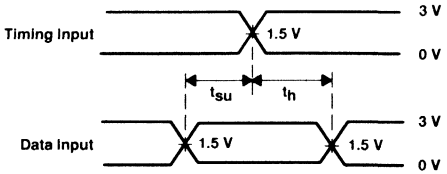
VOLTAGE WAVEFORMS
PULSE DURATION



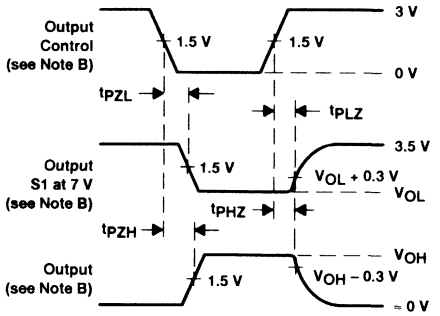
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (A to B)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (B to A)



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES (A port)

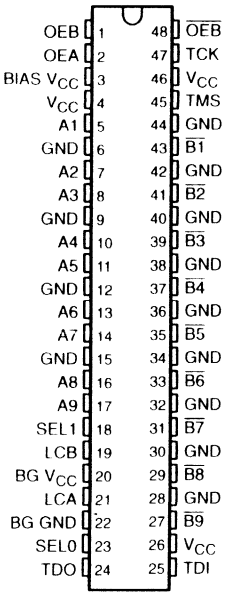
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: TTL inputs – PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns. BTL inputs – PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

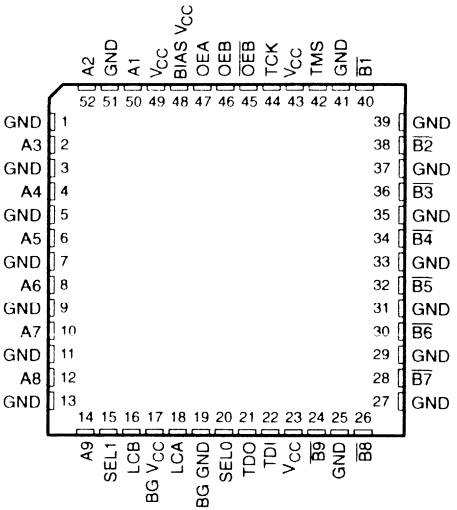
SCBS176D – NOVEMBER 1991 – REVISED MAY 1995

- **Compatible With IEEE 1194.1-1991 (BTL) Standard**
- **TTL A Port, Backplane Transceiver Logic (BTL) $\overline{B}$ Port**
- **Open-Collector $\overline{B}$-Port Outputs Sink 100 mA**
- **Isolated Logic-Ground and Bus-Ground Pins Reduce Noise**
- **BIAS V_{CC} Minimizes Signal Distortion During Live Insertion/Withdrawal**
- **$\overline{B}$-Port Biasing Network Preconditions the Connector and PC Trace to the BTL High-Level Voltage**
- **TTL-Input Structures Incorporate Active Clamping to Aid in Line Termination**
- **Package Options Include Plastic Quad Flat (RC) Package and Ceramic Flat (WD) Package**

SN54FB2031 . . . WD PACKAGE
(TOP VIEW)



SN74FB2031 . . . RC PACKAGE
(TOP VIEW)



description

The 'FB2031 are 9-bit transceivers designed to translate signals between TTL and backplane transceiver logic (BTL) environments. They are specifically designed to be compatible with IEEE 1194.1-1991 (BTL).

The $\overline{B}$ port operates at BTL-signal levels. The open-collector $\overline{B}$ ports are specified to sink 100 mA. Two output enables (OEB and $\overline{OEB}$) are provided for the $\overline{B}$ outputs. When OEB is low, $\overline{OEB}$ is high, or V_{CC} is typically less than 2.5 V, the $\overline{B}$ port is turned off.

description (continued)

The A port operates at TTL-signal levels. The A outputs reflect the inverse of the data at the $\overline{B}$ port when the A-port output enable (OEA) is high. When OEA is low or V_{CC} is typically less than 2.5 V, the A outputs are in the high-impedance state.

Pins are allocated for the 4-wire IEEE 1149.1 (JTAG) test bus. TMS and TCK are not connected and TDI is shorted to TDO.

BIAS V_{CC} establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when V_{CC} is not connected.

BG V_{CC} and BG GND are the supply inputs for the bias generator.

To ensure the high-impedance state during power up or power down, A port should be tied to V_{CC} through a pullup resistor; the minimum value of the resister is determined by the current-sinking capability of the driver.

The SN54FB2031 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74FB2031 is characterized for operation from 0°C to 70°C.

Function Tables

TRANSCEIVER

INPUTS			FUNCTION
OEA	OEB	$\overline{OEB}$	
L	H	L	A data to B bus
H	L	X	$\overline{B}$ data to A bus
H	X	H	
H	H	L	A data to B bus, B data to A bus
L	L	X	Isolation
L	X	H	

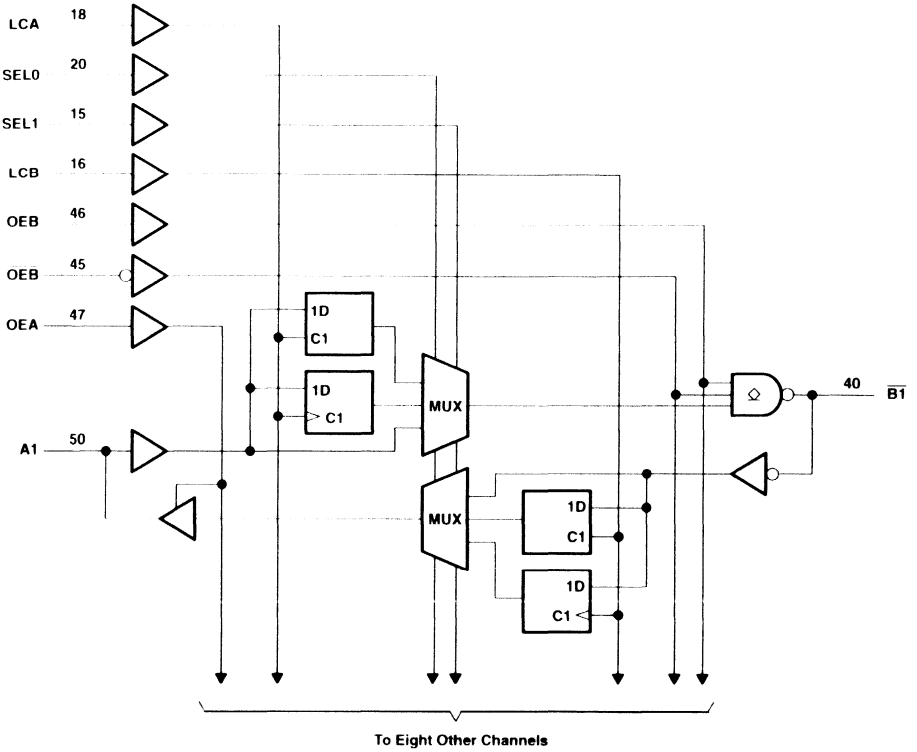
STORAGE MODE

LCA, LCB	RESULT
0	Transparent
1	Latches latched
↑	Flip-flops triggered

SELECT

SEL1	SEL0	MUX A→B	MUX B→A
0	0	Latch	Latch
0	1	Through	Through
1	0	Flip-flop	Flip-flop
1	1	Flip-flop	Latch

functional block diagram



Pin numbers shown are for the RC package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I: except $\overline{B}$ port ..... −1.2 V to 7 V
$\overline{B}$ port ..... −1.2 V to 3.5 V
Input clamp current: except $\overline{B}$ port ..... −40 mA
$\overline{B}$ port ..... −18 mA
Voltage range applied to any $\overline{B}$ output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage range applied to any output in the high state ..... −0.5 V to V_{CC}
Current applied to any single output in the low state: A port ..... 48 mA
$\overline{B}$ port ..... 200 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 1): RC package ..... 1.4 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 75 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 2)

			SN54FB2031			SN74FB2031			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}, BIAS V_{CC}, BG V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	$\overline{B}$ port	1.62*		2.3	1.62		2.3	V
		Except B port	2			2			
V_{IL}	Low-level input voltage	B port	0.75		1.47*	0.75		1.47	V
		Except B port			0.8			0.8	
I_{OH}	High-level output current	A port			−3			−3	mA
I_{OL}	Low-level output current	A port			24			24	mA
		$\overline{B}$ port			100			100	
T_A	Operating free-air temperature		−55		125	0		70	°C

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not tested.

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54FB2031			SN74FB2031			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	B port	V_{CC} = 4.5 V	I_I = –18 mA			–1.2			–1.2	V
	Except B port		I_I = –40 mA			–0.5			–0.5	
V_{OH}	A port	V_{CC} = 4.5 V	I_{OH} = –1 mA		3.2					V
			I_{OH} = –3 mA	2.5	3.3		2.5	3.3		
V_{OL}	A port	V_{CC} = 4.5 V	I_{OL} = 20 mA		0.31					V
			I_{OL} = 24 mA		0.35	0.5		0.35	0.5	
	B port	V_{CC} = 4.5 V	I_{OL} = 80 mA	0.75		1.1	0.75		1.1	
			I_{OL} = 100 mA			1.15			1.15	
I_I	Except B port	V_{CC} = 5.5 V,	V_I = 5.5 V			50			50	µA
I_{IH}‡	Except B port	V_{CC} = 5.5 V,	V_I = 2.7 V			50			50	µA
I_{IL}‡	Except B port	V_{CC} = 5.5 V,	V_I = 0.5 V			–50			–50	µA
	B port	V_{CC} = 5.5 V,	V_I = 0.75 V			–100			–100	
I_{OZH}	A port	V_{CC} = 2.1 V to 5.5 V,	V_O = 2.7 V			50			50	µA
I_{OZL}	A port	V_{CC} = 2.1 V to 5.5 V,	V_O = 0.5 V			–50			–50	µA
I_{OZPU}	A port	V_{CC} = 0 to 2.1 V,	V_O = 0.5 V to 2.7 V			50			50	µA
I_{OZPD}	A port	V_{CC} = 2.1 V to 0,	V_O = 0.5 V to 2.7 V			–50			–50	µA
I_{OH}	B port	V_{CC} = 0 to 5.5 V,	V_O = 2.1 V			100			100	µA
I_{OS}§	A port	V_{CC} = 5.5 V,	V_O = 0	–30		–150	–30		–150	mA
I_{CC}	A port to B port	V_{CC} = 5.5 V,	I_O = 0			78			78	mA
	B port to A port					78			78	
C_i		V_I = 0.5 V or 2.5 V			4.5			4.5		pF
C_{io}¶	A port	V_O = 0.5 V or 2.5 V			8.5			8.5		pF
	B port per P1194.0	V_{CC} = 0 to 5.5 V				6			6	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
¶ Parameter is based on characterization but is not tested.

live-insertion specifications over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		SN54FB2031		SN74FB2031		UNIT
				MIN	MAX	MIN	MAX	
I_{CC} (BIAS V_{CC})		V_{CC} = 0 to 4.5 V	V_B = 0 to 2 V, V_I (BIAS V_{CC}) = 4.5 V to 5.5 V		450		450	µA
		V_{CC} = 4.5 V to 5.5 V			10		10	
V_O	B port	V_{CC} = 0,	V_I (BIAS V_{CC}) = 5 V	1.62	2.1	1.62	2.1	V
I_O	B port	V_{CC} = 0,	V_B = 1 V, V_I (BIAS V_{CC}) = 4.5 V to 5.5 V		10	–1		µA
		V_{CC} = 0 to 5.5 V,	OEB = 0 to 0.8 V		100		100	
		V_{CC} = 0 to 2.2 V,	OEB = 0 to 5 V		100		100	

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

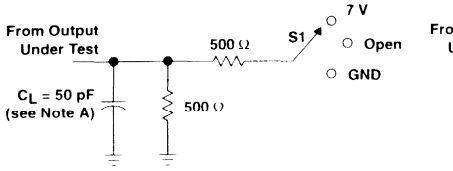
		SN54FB2031		SN74FB2031		UNIT
		MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	150	0	150	MHz
t_w	Pulse duration, LCA or LCB	3.3		3.3		ns
t_{su}	Setup time, data before LCA↑ (clock mode)	1.5		1.4		ns
	Setup time, data before LCB↑ (clock mode)	2.8		2.8		
	Setup time, data before LCA↑ (latch mode)	1.1		1.1		
	Setup time, data before LCB↑ (latch mode)	2.4		2.4		
t_h	Hold time, data after LCA↑ (clock mode)	0.6		0.6		ns
	Hold time, data after LCB↑ (clock mode)	0		0		
	Hold time, data after LCA↑ (latch mode)	0.9		0.9		
	Hold time, data after LCB↑ (latch mode)	0		0		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

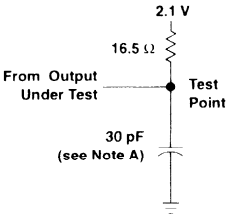
PARAMETER		FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54FB2031		SN74FB2031		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
f_{max}						150		150		150	MHz
t_{PLH}		A (through mode)	$\overline{B}$	3.7	4.5	5.9	3.2	8	3.2	6.6	ns
t_{PHL}				2.9	4	5.7	2.6	7.8	2.6	5.9	
t_{PLH}		A (transparent)	B	4.1	5	6.5	3.6	8.6	3.6	7.3	ns
t_{PHL}				3.3	4.5	6.1	3	8.3	3	6.5	
t_{PLH}		LCA	B	4.5	5.4	7	3.9	9.1	3.9	7.8	ns
t_{PHL}				4	5.1	6.7	3.4	9	3.4	7.4	
t_{PLH}		LCB	A	2.8	3.7	4.7	1.9	7.9	1.9	6	ns
t_{PHL}				2.5	3.4	4.9	1.8	7.4	1.8	5.5	
t_{PLH}		SEL1 or SEL0	A	2.5	3.8	5.3	1.9	7.9	1.9	6.3	ns
t_{PHL}				2.2	3.5	5.1	1.6	7.1	1.6	5.6	
t_{PLH}		SEL1 or SEL0	B	4.1	5.3	6.9	3.7	8.3	3.7	7.8	ns
t_{PHL}				3.7	5.2	6.9	3.3	9.2	3.3	7.7	
t_{PLH}		B (through mode)	A	3.1	4	5.6	2.2	8.6	2.2	7.1	ns
t_{PHL}				2.6	3.4	4.9	1.4	7.6	1.4	5.7	
t_{PLH}		$\overline{B}$ (transparent)	A	3.3	4.2	5.9	2.4	9	2.4	7.6	ns
t_{PHL}				2.8	3.9	5.5	1.8	8.2	1.8	6.3	
t_{PLH}		OEB or $\overline{OEB}$	B	3.7	4.6	6.1	3.2	8.4	3.2	6.7	ns
t_{PHL}				2.9	4.3	5.8	2.5	8.2	2.5	6.4	
t_{PZH}		OEA	A	2.3	3.1	4.5	1.6	7.3	1.6	5	ns
t_{PZL}				1.9	2.7	4.1	1.6	7	1.6	4.4	
t_{PHZ}		OEA	A	2.2	3.1	4.5	1.5	7.1	1.5	5.2	ns
t_{PLZ}				2.5	3.3	4.9	2	7.2	2	5.2	
$t_{sk(p)}$	Skew for any single channel $\lvert t_{PHL} - t_{PLH} \rvert$	A	$\overline{B}$		0.5						ns
		$\overline{B}$	A		0.3						
$t_{sk(o)}$	Skew between drivers in the same package	A	$\overline{B}$		0.2						ns
		$\overline{B}$	A		0.3						
t_t	Transition time, B outputs (1.3 V to 1.8 V)			0.6	2	2.8	0.3	3.3	0.4	2.9	ns
	Transition time, A outputs (10% to 90%)			0.5	3.5	4.7	0	6.4	0	5.4	
B-port input pulse rejection				1			1		1		ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

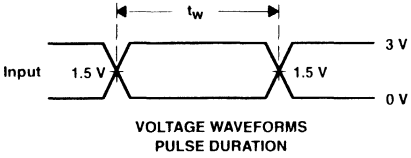


LOAD CIRCUIT FOR A OUTPUTS

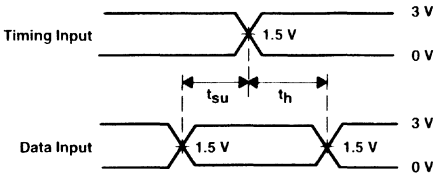


LOAD CIRCUIT FOR B OUTPUTS

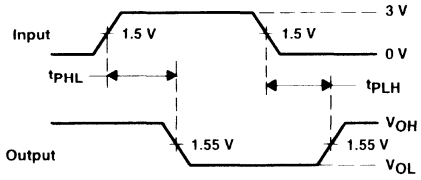
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	GND



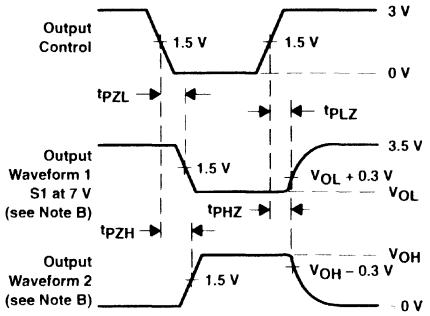
VOLTAGE WAVEFORMS
PULSE DURATION



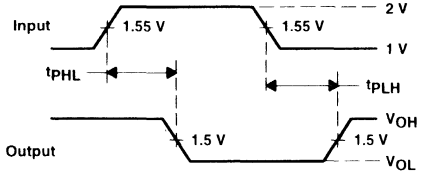
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (A to B)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES (A port)



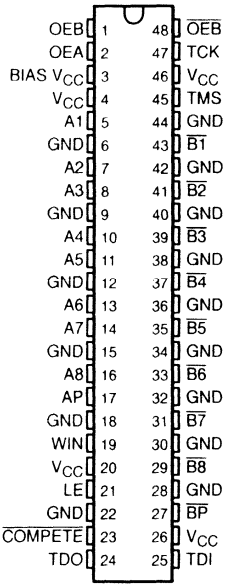
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (B to A)

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: TTL inputs – PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns. BTL inputs – PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

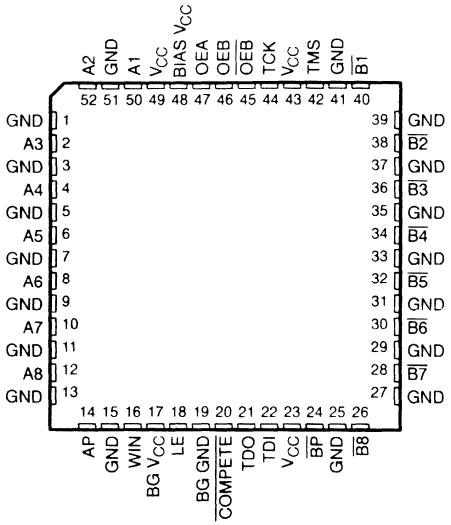
Figure 1. Load Circuits and Voltage Waveforms

- Compatible With IEEE 1194.1-1991 (BTL) and IEEE 896.2-1991 (Futurebus+) Standards
- TTL A Port, Backplane Transceiver Logic $\overline{B}$ Port
- Open-Collector $\overline{B}$-Port Outputs Sink 100 mA
- Minimum $\overline{B}$-Port Edge Rate = 2 ns
- Isolated Logic-Ground and Bus-Ground Pins Reduce Noise
- BIAS V_{CC} Pin Minimizes Signal Distortion During Live Insertion/Withdrawal
- $\overline{B}$-Port Biasing Network Preconditions the Connector and PC Trace to the Backplane Transceiver Logic High-Level Voltage
- TTL-Input Structures Incorporate Active Clamping Networks to Aid in Line Termination
- Package Options Include Plastic Quad Flat (RC) Package and Ceramic Flat (WD) Package

SN54FB2032 . . . WD PACKAGE
(TOP VIEW)



SN74FB2032 . . . RC PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

The 'FB2032 are 9-bit transceivers designed to translate signals between TTL and backplane transceiver logic (BTL) environments and to perform bus arbitration. They are specifically designed to be compatible with IEEE 1194.1-1991 (BTL) and IEEE 896.2-1991 (Futurebus+) standards.

The $\overline{B}$ port operates at BTL-signal levels. The open-collector $\overline{B}$ ports are specified to sink 100 mA and have minimum output edge rates of 2 ns. Two output enables, OEB and $\overline{OEB}$, are provided for the $\overline{B}$ outputs. When OEB is low, $\overline{OEB}$ is high, or V_{CC} is typically less than 2.5 V, the $\overline{B}$ port is turned off.

description (continued)

The A port operates at TTL-signal levels. The A outputs reflect the inverse of the data at the $\overline{B}$ port when the A-port output enable, OEA, is high. When OEA is low or when V_{CC} is typically less than 2.5 V, the A outputs are in the high-impedance state.

The A-port data can be latched by taking the latch enable (LE) high. When LE is low, the latches are transparent.

The Futurebus+ protocol logic can be activated by taking $\overline{\text{COMPETE}}$ low. The module (device) then compares its A data (arbitration number) against the A data of another identical module also connected to the $\overline{B}$ arbitration bus, and sets WIN high if the A data is greater than the A data of the other module (i.e., has higher priority). A8 and $\overline{B8}$ are the most significant bits, and A1 and $\overline{B1}$ are the least significant bits. If OEB is high and $\overline{OEB}$ is low during this operation and the A bus of the first module wins priority, the A bus asserts its arbitration number on the $\overline{B}$-arbitration bus.

AP and $\overline{BP}$ are the bus-parity bits. The winning module may assert $\overline{BP}$ low if its parity bit (AP) is high.

In a typical operating sequence, a Futurebus+ arbitration controller latches its arbitration number into the A port and waits for the results of a competition. When the competition is complete, and if the controller's arbitration number did not win, the controller reads back the current value of the $\overline{B}$ bus (by taking OEA high) and determines the winning arbitration number. This allows the module to change its arbitration number for the next competition cycle, if desired.

Pins are allocated for the four-wire IEEE 1149.1 (JTAG) test bus, which will be implemented in a future version of the 'FB2032. Currently, TMS and TCK are not connected and TDI is shorted to TDO.

BIAS V_{CC} establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when V_{CC} is not connected.

BG V_{CC} and BG GND are the supply inputs for the bias generator.

The SN54FB2032 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74FB2032 is characterized for operation from 0°C to 70°C.

Function Tables

TRANSCEIVER

INPUTS			FUNCTION
OEA	OEB	$\overline{OEB}$	
L	H	L	$\overline{A}$ data to B bus
H	L	X	$\overline{B}$ data to A bus
H	X	H	
H	H	L	$\overline{A}$ data to B bus, $\overline{B}$ data to A bus
L	L	X	Isolation
L	X	H	

WIN

INPUTS				WIN
OEB	$\overline{OEB}$	$\overline{COMPETE}$	DATA A1, A2†	
H	H	X	X	L
H	L	H	X	L
H	L	L	A1 < A2	L
H	L	L	A2 ≤ A1	H

† A1 refers to the A data of Module 1 and A2 refers to the A data of Module 2. If LE = L, A = current A data. If LE = H, A = the value of A8-A1 prior to the most recent low-to-high transition of LE.

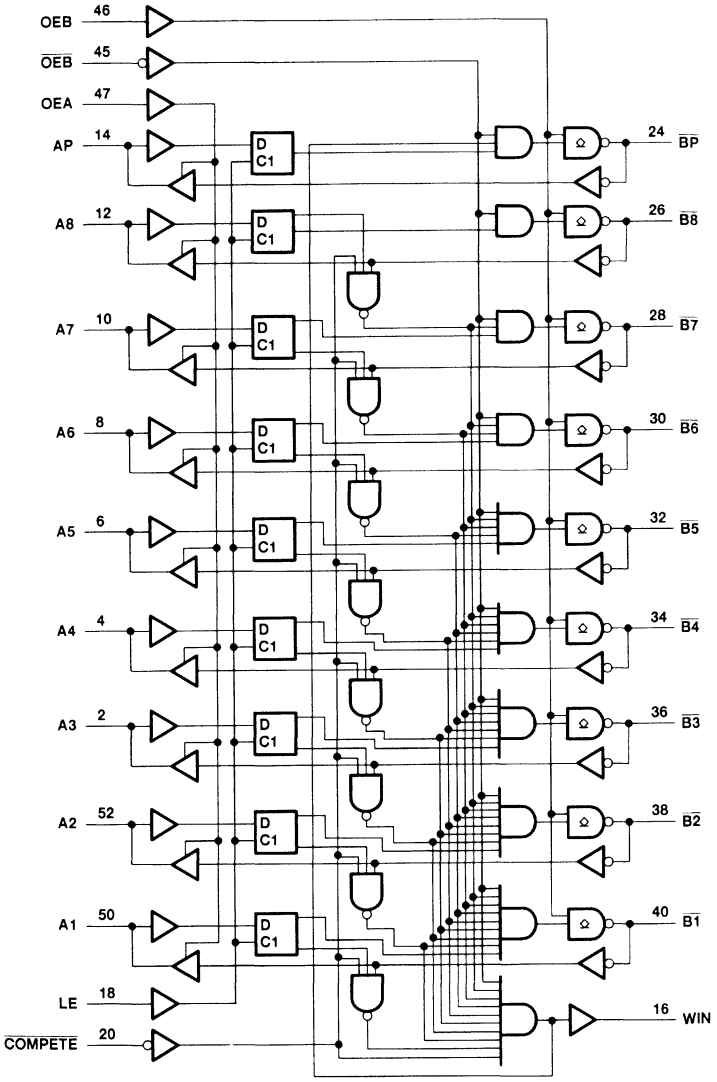
$\overline{BP}$

INPUTS				BP
OEB	$\overline{OEB}$	WIN	AP‡	
L	X	X	X	H
X	H	X	X	H
H	L	L	X	H
H	L	H	L	H
H	L	H	H	L

‡ If LE = L, AP = current AP data, if LE = H, AP = the level of AP prior to the most recent low-to-high transition of LE.

PRODUCT PREVIEW

functional block diagram



Pin numbers shown are for the RC package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I: except $\overline{BP}$, $\overline{B}$ port ..... −1.2 V to 7 V
$\overline{BP}$, $\overline{B}$ port ..... −1.2 V to 3.5 V
Input current range (except $\overline{B}$ port) ..... −40 mA to 5 mA
Voltage range applied to any $\overline{B}$ output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage range applied to any output in the high state ..... −0.5 V to V_{CC}
Current applied to any single output in the low state: A port ..... 48 mA
$\overline{B}$ port ..... 200 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 1): RC package ..... 1.4 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 75 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 2)

			SN54FB2032			SN74FB2032			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}, BIAS V_{CC}, BG V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	$\overline{BP}$, $\overline{B}$ port	1.62		2.3	1.62		2.3	V
		Except $\overline{B}$ port	2			2			
V_{IL}	Low-level input voltage	$\overline{BP}$, $\overline{B}$ port	0.75		1.47	0.75		1.47	V
		Except $\overline{B}$ port			0.8			0.8	
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	High-level output current	AP, WIN, A port						−3	mA
I_{OL}	Low-level output current	AP, WIN, A port						24	mA
		$\overline{BP}$, $\overline{B}$ port			100			100	
T_A	Operating free-air temperature		−55		125	0		70	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54FB2032			SN74FB2032			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$\overline{BP}$, $\overline{B}$ port	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
	Except $\overline{BP}$, $\overline{B}$ port	V_{CC} = 4.5 V,	I_I = −40 mA			−0.5			−0.5	
V_{OH}	AP, WIN, A port	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.5	3.3		2.5	3.3		V
V_{OL}	AP, WIN, A port	V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.35	0.5		0.35	0.5	V
	$\overline{BP}$, $\overline{B}$ port	V_{CC} = 4.5 V,	I_{OL} = 80 mA	0.75		1.1	0.75		1.1	
I_I	Except $\overline{BP}$, $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 5.5 V			50			50	μA
I_{IH}‡	Except $\overline{BP}$, $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 2.7 V			50			50	μA
I_{IL}‡	Except $\overline{BP}$, $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 0.5 V			−50			−50	μA
	$\overline{BP}$, $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 0.75 V			−100			−100	
I_{OH}	$\overline{BP}$, $\overline{B}$ port	V_{CC} = 0 to 5.5 V,	V_O = 2.1 V			100			100	μA
I_{OS}§	AP, WIN, A port	V_{CC} = 5.5 V,	V_O = 0	−30		−150	−30		−150	mA
I_{CC}	A port to $\overline{B}$ port	V_{CC} = 5.5 V,	I_O = 0		25			25		mA
	$\overline{B}$ port to A port				60			60		
C_i		V_I = V_{CC} or GND				5			5	pF
C_o	A port	V_O = V_{CC} or GND								pF
C_{io}	$\overline{B}$ port per P1194.0	V_{CC} = 0 to 4.5 V				6			6	pF
		V_{CC} = 4.5 V to 5.5 V				5			5	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

live-insertion specifications over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		SN54FB2032		SN74FB2032		UNIT
				MIN	MAX	MIN	MAX	
I_{CC} (BIAS V_{CC})		V_{CC} = 0 to 4.5 V	V_B = 0 to 2 V, V_I (BIAS V_{CC}) = 4.5 V to 5.5 V		450		450	μA
		V_{CC} = 4.5 V to 5.5 V			10		10	
V_O	$\overline{B}$ port	V_{CC} = 0,	V_I (BIAS V_{CC}) = 4.5 V to 5.5 V	1.62	2.1	1.62	2.1	V
I_O	$\overline{B}$ port	V_{CC} = 0,	V_B = 1 V, V_I (BIAS V_{CC}) = 4.5 V to 5.5 V	−1		−1		μA
		V_{CC} = 0 to 5.5 V,	OEB = 0 to 0.8 V		100		100	
		V_{CC} = 0 to 2.2 V,	OEB = 0 to 5 V		100		100	

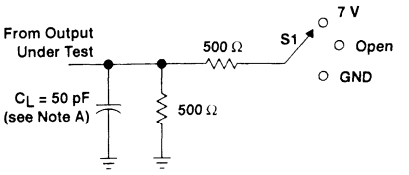
PRODUCT PREVIEW

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

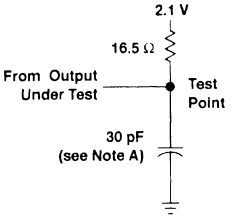
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C	SN54FB2032		SN74FB2032		UNIT
			MIN MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or AP	B or $\overline{BP}$			8		8	ns
t_{PHL}					8		8	
t_{PLH}	A	$\overline{B}_{n-1}$			9		9	ns
t_{PHL}					9		9	
t_{PLH}	A	$\overline{BP}$			10		10	ns
t_{PHL}					10		10	
t_{PLH}	$\overline{B}$	$\overline{B}_{n-1}$			9		9	ns
t_{PHL}					9		9	
t_{PLH}	LE	$\overline{B}$			7.5		7.5	ns
t_{PHL}					7.5		7.5	
t_{PLH}	LE	$\overline{BP}$			7.5		7.5	ns
t_{PHL}					7.5		7.5	
t_{PLH}	$\overline{B}$ or $\overline{BP}$	A or AP			7.5		7.5	ns
t_{PHL}					7.5		7.5	
t_{PLH}	$\overline{B}$	WIN			8.5		8.5	ns
t_{PHL}					8.5		8.5	
t_{PLH}	A	WIN			7.6		7.6	ns
t_{PHL}					7.6		7.6	
t_{PLH}	LE	WIN			7		7	ns
t_{PHL}					7		7	
t_{PLH}	$\overline{COMPETE}$	WIN			5.5		5.5	ns
t_{PHL}					5.5		5.5	
t_{PLH}	$\overline{OEB}$	WIN			6		6	ns
t_{PHL}					6		6	
t_{PLH}	$\overline{COMPETE}$	$\overline{B}$			7.5		7.5	ns
t_{PHL}					7.5		7.5	
t_{PLH}	$\overline{COMPETE}$	$\overline{BP}$			6.5		6.5	ns
t_{PHL}					6.5		6.5	
t_{PLH}	OEB	$\overline{B}$			6.5		6.5	ns
t_{PHL}					6.5		6.5	
t_{PLH}	$\overline{OEB}$	$\overline{B}$			6.5		6.5	ns
t_{PHL}					6.5		6.5	
t_{PZH}	OEA	A			5.5		5.5	ns
t_{PZL}					5.5		5.5	
t_{PHZ}	OEA	A			7		7	ns
t_{PLZ}					7		7	
t_t	Transition time, $\overline{B}$ outputs (1.3 V to 1.8 V)		2	1	3	1	3	ns
t_{PR}	$\overline{B}$-port input pulse rejection				1		1	ns

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

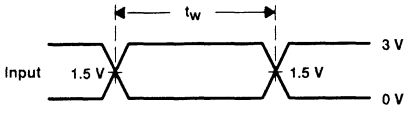


LOAD CIRCUIT FOR A OUTPUTS

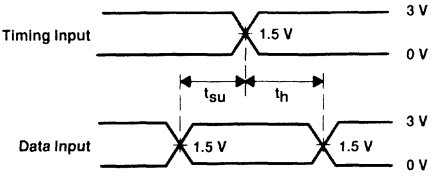


LOAD CIRCUIT FOR B OUTPUTS

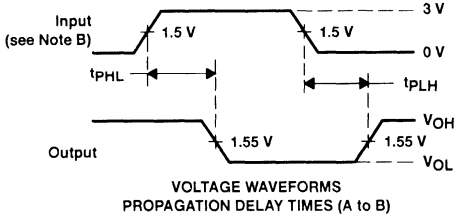
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	GND



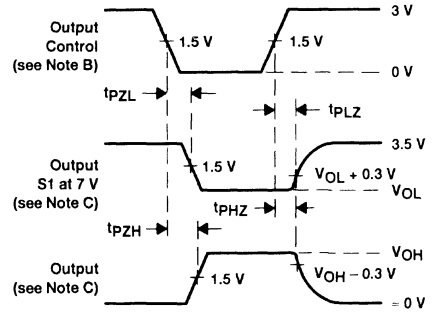
VOLTAGE WAVEFORMS
PULSE DURATION



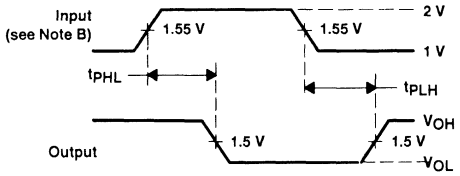
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (A to B)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES (A port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (B to A)

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: TTL inputs – PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns. BTL inputs – PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PRODUCT PREVIEW

- TTL A Port, Backplane Transceiver Logic (BTL) $\overline{B}$ Port
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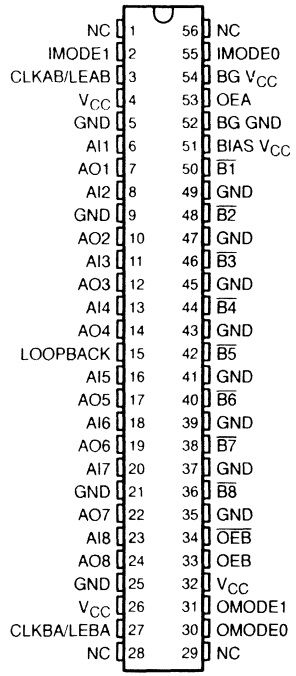
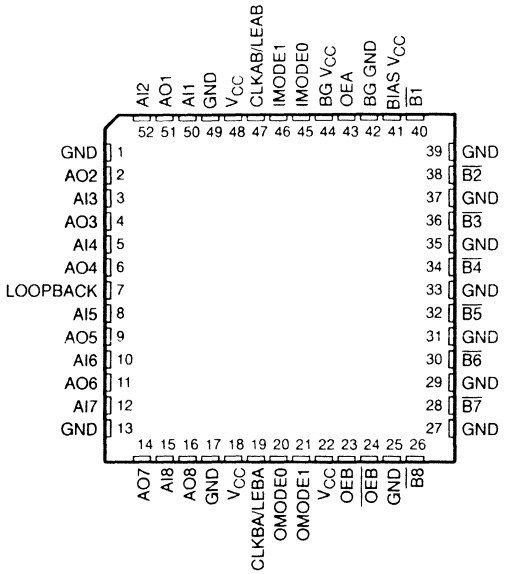
- TTL-Input Structures Incorporate Active Clamping Networks to Aid in Line Termination
- Package Options Include Plastic Quad Flat (RC) Package and Ceramic Flat (WD) Package

SN54FB2033 . . . WD PACKAGE
(TOP VIEW)



NC – No internal connection

SN74FB2033A . . . RC PACKAGE
(TOP VIEW)



TEXAS INSTRUMENTS

description

The SN54FB2033 and SN74FB2033A are 8-bit transceivers featuring a split input (AI) and output (AO) bus on the TTL-level A port. The common-I/O, open-collector $\overline{B}$ port operates at backplane transceiver logic (BTL) signal levels.

The logic element for data flow in each direction is configured by two mode inputs (IMODE1 and IMODE0 for B-to-A, OMODE1 and OMODE0 for A-to-B) as a buffer, a D-type flip-flop, or a D-type latch. When configured in the buffer mode, the inverted input data appears at the output port. In the flip-flop mode, data is stored on the rising edge of the appropriate clock input (CLKAB/LEAB or CLKBA/LEBA). In the latch mode, the clock pins serve as active-high transparent latch enables.

Data flow in the B-to-A direction, regardless of the logic element selected, is further controlled by the LOOPBACK input. When LOOPBACK is low, $\overline{B}$-port data is the B-to-A input. When LOOPBACK is high, the output of the selected A-to-B logic element (prior to inversion) is the B-to-A input.

The AO port-enable/-disable control is provided by OEA. When OEA is low or when V_{CC} is less than 2.5 V, the AO port is in the high-impedance state. When OEA is high, the AO port is active (high or low logic levels).

The $\overline{B}$ port is controlled by $\overline{OEB}$ and $\overline{OEB}$. If OEB is low, $\overline{OEB}$ is high, or V_{CC} is less than 2.5 V, the $\overline{B}$ port is inactive. If OEB is high and $\overline{OEB}$ is low, the B port is active.

BG V_{CC} and BG GND are the bias-generator reference inputs.

The A-to-B and B-to-A logic elements are active regardless of the state of their associated outputs. The logic elements can enter new data (in flip-flop and latch modes) or retain previously stored data while the associated outputs are in the high-impedance (AO port) or inactive ($\overline{B}$ port) states.

Output clamps are provided on the BTL outputs to reduce switching noise. One clamp reduces inductive ringing effects on V_{OH} during a low-to-high transition. The other clamps out ringing below the BTL V_{OL} voltage of 0.75 V. Both these clamps are active only during AC switching and do not affect the BTL outputs during steady-state conditions.

BIAS V_{CC} establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when V_{CC} is not connected.

The SN54FB2033 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74FB2033A is characterized for operation from 0°C to 70°C.

Function Tables

FUNCTION/MODE TABLE

INPUTS								FUNCTION/MODE
OEA	OEB	$\overline{OEB}$	OMODE1	OMODE0	IMODE1	IMODE0	LOOPBACK	
L	L	X	X	X	X	X	X	Isolation
L	X	H	X	X	X	X	X	
X	H	L	L	L	X	X	X	AI to $\overline{B}$, buffer mode
X	H	L	L	H	X	X	X	AI to $\overline{B}$, flip-flop mode
X	H	L	H	X	X	X	X	AI to $\overline{B}$, latch mode
H	L	X	X	X	L	L	L	$\overline{B}$ to AO, buffer mode
H	X	H	X	X	L	L	L	
H	L	X	X	X	L	H	L	$\overline{B}$ to AO, flip-flop mode
H	X	H	X	X	L	H	L	
H	L	X	X	X	H	X	L	$\overline{B}$ to AO, latch mode
H	X	H	X	X	H	X	L	
H	L	X	X	X	L	L	H	AI to AO, buffer mode
H	X	H	X	X	L	L	H	
H	L	X	X	X	L	H	H	AI to AO, flip-flop mode
H	X	H	X	X	L	H	H	
H	L	X	X	X	H	X	H	AI to AO, latch mode
H	X	H	X	X	H	X	H	
H	H	L	X	X	X	X	L	AI to $\overline{B}$, $\overline{B}$ to AO

Function Tables (Continued)

ENABLE/DISABLE

INPUTS			OUTPUTS	
OEA	OEB	$\overline{OEB}$	AO	B
L	X	X	Hi Z	
H	X	X	Active	
X	L	L		Inactive (H)
X	L	H		Inactive (H)
X	H	L		Active
X	H	H		Inactive (H)

BUFFER

INPUT	OUTPUT
L	H
H	L

LATCH

INPUTS		OUTPUT
CLK/LE	DATA	
H	L	H
H	H	L
L	X	Q_0

LOOPBACK

LOOPBACK	Q†
L	$\overline{B}$ port
H	Point P‡

† Q is the input to the B-to-A logic element.
‡ P is the output of the A-to-B logic element (see functional block diagram).

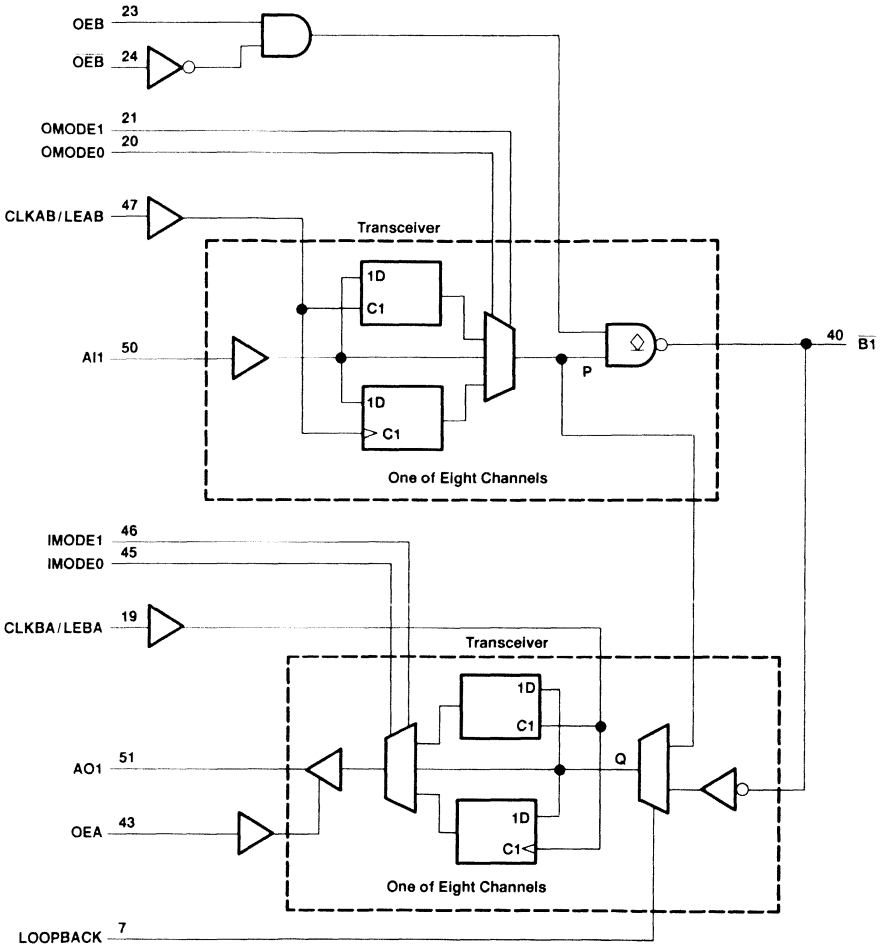
SELECT

INPUTS		SELECTED LOGIC ELEMENT
MODE1	MODE0	
L	L	Buffer
L	H	Flip-flop
H	X	Latch

FLIP-FLOP

INPUTS		OUTPUT
CLK/LE	DATA	
L	X	Q_0
↑	L	H
↑	H	L

functional block diagram



Pin numbers shown are for the RC package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I: except $\overline{B}$ port ..... –1.2 V to 7 V
$\overline{B}$ port ..... –1.2 V to 3.5 V
Input current range, (except $\overline{B}$ port) ..... –40 mA to 5 mA
Voltage range applied to any B output in the disabled or power-off state ..... –0.5 V to 3.5 V
Voltage range applied to any output in the high state: A port ..... –0.5 V to V_{CC}
Current applied to any single output in the low state: A port ..... 48 mA
$\overline{B}$ port ..... 200 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 1): RC package ..... 1.4 W
Storage temperature range ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 75 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 2)

			SN54FB2033			SN74FB2033A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}, BG V_{CC}	Supply voltage		4.75	5	5.25	4.75	5	5.25	V
BIAS V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	$\overline{B}$ port	1.62*		2.3	1.62		2.3	V
		Except $\overline{B}$ port	2			2			
V_{IL}	Low-level input voltage	$\overline{B}$ port	0.75		1.47*	0.75		1.47	V
		Except $\overline{B}$ port			0.8			0.8	
I_{OH}	High-level output current	AO port			–3			–3	mA
I_{OL}	Low-level output current	AO port			24			24	mA
		$\overline{B}$ port			100			100	
$\Delta t/\Delta v$	Input transition rise or fall rate	Except $\overline{B}$ port			10			10	ns/V
T_A	Operating free-air temperature		–55		125	0		70	°C

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not tested.

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54FB2033			SN74FB2033A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.75 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	AO port	V_{CC} = 4.75 V to 5.25 V,	I_{OH} = −10 μA			V_{CC}−1			V_{CC}−1.1	V
		V_{CC} = 4.75 V	I_{OH} = −3 mA	2.5	2.85	3.4	2.5	2.85	3.4	
			I_{OH} = −32 mA	2			2			
V_{OL}	AO port	V_{CC} = 4.75 V	I_{OL} = 20 mA		0.33	0.5		0.33	0.5	V
			I_{OL} = 55 mA			0.8			0.8	
	B port	V_{CC} = 4.75 V	I_{OL} = 100 mA	0.75		1.1	0.75		1.1	
			I_{OL} = 4 mA	0.5			0.5			
I_I	Except B port	V_{CC} = 0,	V_I = 5.25 V			100			100	μA
I_{IH}	Except $\overline{B}$ port	V_{CC} = 5.25 V,	V_I = 2.7 V			50			50	μA
	$\overline{B}$ port‡	V_{CC} = 0 to 5.25 V,	V_I = 2.1 V			100			100	
I_{IL}	Except $\overline{B}$ port	V_{CC} = 5.25 V,	V_I = 0.5 V			−50			−50	μA
	$\overline{B}$ port‡	V_{CC} = 5.25 V,	V_I = 0.75 V			−100			−100	
I_{OH}	B port	V_{CC} = 0 to 5.25 V,	V_O = 2.1 V			100			100	μA
I_{OZH}	AO port	V_{CC} = 5.25 V,	V_O = 2.7 V			50			50	μA
I_{OZL}	AO port	V_{CC} = 5.25 V,	V_O = 0.5 V			−50			−50	μA
I_{OS}§	AO port	V_{CC} = 5.25 V,	V_O = 0	−40	−80	−150	−40	−80	−150	mA
I_{CC}	All outputs on	V_{CC} = 5.25 V,	I_O = 0		45	90		45	70	mA
C_i	AI port and control inputs	V_I = V_{CC} or GND			5			5		pF
C_o	AO port	V_O = V_{CC} or GND			5			5		pF
C_{io}¶	$\overline{B}$ port per P1194.0	V_{CC} = 0 to 4.75 V				8			6	pF
		V_{CC} = 4.75 V to 5.25 V				8			6	

† All typical values are at V_{CC} = 5 V.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
¶ Parameter is based on characterization data but is not tested.

live-insertion characteristics over recommended operating free-air temperature range (see Note 3)

PARAMETER		TEST CONDITIONS		SN54FB2033		SN74FB2033A		UNIT
				MIN	MAX	MIN	MAX	
I_{CC} (BIAS V_{CC})		V_{CC} = 0 to 4.5 V	V_B = 0 to 2 V, V_I (BIAS V_{CC}) = 4.5 V to 5.5 V		400		400	μA
		V_{CC} = 4.5 V to 5.5 V			10		10	
V_O	$\overline{B}$ port	V_{CC} = 0,	V_I (BIAS V_{CC}) = 4.5 V to 5.5 V	1.62	2.1	1.62	2.1	V
I_O	$\overline{B}$ port	V_{CC} = 0,	V_B = 1 V, V_I (BIAS V_{CC}) = 4.5 V to 5.5 V	−30		−1		μA
		V_{CC} = 0 to 5.5 V,	OEB = 0 to 0.8 V		170		100	
		V_{CC} = 0 to 2.2 V,	OEB = 0 to 5 V		100		100	

NOTE 3: Power-up sequence is as follows: GND, BIASV_{CC}, V_{CC}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)

		SN54FB2033				SN74FB2033A				UNIT
		V_{CC} = 5 V, T_A = 25°C		MIN	MAX	V_{CC} = 5 V, T_A = 25°C		MIN	MAX	
		MIN	MAX			MIN	MAX			
f_{clock}	Clock frequency	0	150	0	150	0	150	0	150	MHz
t_w	Pulse duration, CLKAB/LEAB or CLKBA/LEBA	3.9		4.3		3.3		3.3		ns
t_{su}	Setup time, data before CLKAB/LEAB or CLKBA/LEBA↑	2.9		3.3		2.7		2.7		ns
t_h	Hold time, data after CLKAB/LEAB or CLKBA/LEBA↑	1		1.3		0.7		0.7		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54FB2033					SN74FB2033A					UNIT
			V_{CC} = 5 V, T_A = 25°C			MIN	MAX	V_{CC} = 5 V, T_A = 25°C			MIN	MAX	
			MIN	TYP	MAX			MIN	TYP	MAX			
f_{max}			150			150		150			150		MHz
t_{PLH}	AI (thru mode)	$\overline{B}$	1.7	3.8	4.6	1.2	7.5	2.3	3.6	4.6	2.3	5.6	ns
t_{PHL}			1.3	2.6	4.3	1	5.5	1.9	3	4.2	1.9	4.5	
t_{PLH}	$\overline{B}$ (thru mode)	AO	2.5	3.9	5.9	1.4	7.6	2.5	4.2	5.5	2.5	6.1	ns
t_{PHL}			2.7	5.2	5.7	1.6	7.8	3	4.2	5.6	3	5.7	
t_{PLH}	AI (transparent)	$\overline{B}$	1.7	5	4.6	1.2	8.7	2.3	3.6	4.6	2.3	5.6	ns
t_{PHL}			1.3	3.6	4.3	1	5.9	1.9	3	4.1	1.9	4.5	
t_{PLH}	$\overline{B}$ (transparent)	AO	2.5	4.3	5.8	1.5	7.8	2.5	4.2	5.5	2.5	6.1	ns
t_{PHL}			2.7	5.6	5.7	1.6	8	3	4.2	5.6	3	5.7	
t_{PLH}	OEB	$\overline{B}$	1.6	3.7	4.7	1.1	6.6	2.4	3.7	4.7	2.4	5.8	ns
t_{PHL}			1.2	2.6	4.1	0.4	5.4	1.8	3	4.1	1.8	4.4	
t_{PLH}	$\overline{OEB}$	$\overline{B}$	1.3	3.8	4.3	1.2	6.6	2	3.4	4.3	2	5.2	ns
t_{PHL}			1.2	2.9	4.4	0.8	5.5	2	3.3	4.4	2	4.8	
t_{PZH}	OEA	AO	2	3.5	5.1	1.2	6.6	2	3.5	4.6	2	5.1	ns
t_{PZL}			2.7	4.3	6.1	1.3	7.7	2.7	4.2	5.1	2.7	5.4	
t_{PHZ}	OEA	AO	2.1	3.5	5.8	1.1	6.9	2.1	4	5	2.1	5.5	ns
t_{PLZ}			1.6	2.7	4.7	1	6	1.6	2.8	3.9	1.6	4.3	
t_{PLH}	CLKAB/LEAB	$\overline{B}$	2.1	5	5.8	1.6	8.7	3	4.7	5.8	3	6.9	ns
t_{PHL}			2	3.6	5.6	1.1	6.6	2.8	4.3	5.6	2.8	6.1	
t_{PLH}	CLKBA/LEBA	AO	2	3.8	5.4	1.4	6.7	2	3.6	4.9	2	5.4	ns
t_{PHL}			2.2	4.1	5.6	1.5	6.5	2.2	3.5	4.7	2.2	5.1	
t_{PLH}	OMODE	$\overline{B}$	2.3	4.8	6.1	1.6	8.1	2.4	5	6.1	2.4	7.2	ns
t_{PHL}			1.4	3.5	6	1	6.5	2.4	4.5	6	2.4	6.7	
t_{PLH}	IMODE	AO	1.8	3.6	5.9	1.3	7.3	1.8	4	5.3	1.8	5.9	ns
t_{PHL}			2.3	4.1	5.4	1.4	6.4	2.3	4.1	5.2	2.3	5.4	
t_{PLH}	LOOPBACK	AO	2.4	4.6	7.1	1.6	8.3	2.4	5	7	2.4	8	ns
t_{PHL}			3.1	4.8	6.9	1.8	7.5	3.1	4.6	5.7	3.1	5.9	
t_{PLH}	AI	AO	1.9	3.7	5.7	1.4	7.1	1.9	3.7	5.5	1.9	6.1	ns
t_{PHL}			2.6	4.3	5.8	1.6	7.3	2.6	4.2	5.6	2.6	5.8	
t_t	Rise time, 1.3 V to 1.8 V	$\overline{B}$	0.5	1.5	2.1	0.4	3.2	0.5	1.2	2.1	0.5	3	ns
	Fall time, 1.8 V to 1.3 V		0.4	1.5	2.3	0.4	3.4	0.5	1.4	2.3	0.5	3	
	Rise time, 10% to 90%	AO	2	3.5	4.2	1.8	5.4	2	3.3	4.2	2	5	
	Fall time, 90% to 10%		1	2.5	3.4	0.8	5.1	1	2.5	3.4	1	5	
t_{PR}	$\overline{B}$-port input pulse rejection					1*					1		ns

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not tested.

output-voltage characteristics

PARAMETER			TEST CONDITIONS	SN54FB2033		SN74FB2033A		UNIT
				MIN	MAX	MIN	MAX	
V_{OHP}†	Peak output voltage during turnoff of 100 mA into 40 nH	$\overline{B}$ port	See Figure 1		4		4.5	V
V_{OHV}†	Minimum output voltage during turnoff of 100 mA into 40 nH			1.62		1.62		V
V_{OLV}	Minimum output voltage during high-to-low switch		I_{OL} = −50 mA	0.3		0.3		V

† Parameter is based on characterization data but not tested.

PARAMETER MEASUREMENT INFORMATION

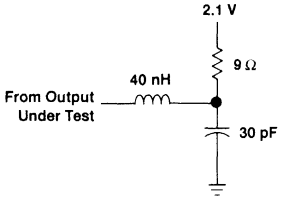
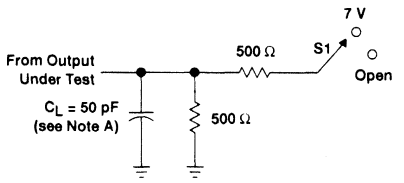
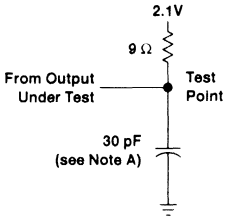


Figure 1. Load Circuit for V_{OHP}, V_{OHV}

PARAMETER MEASUREMENT INFORMATION

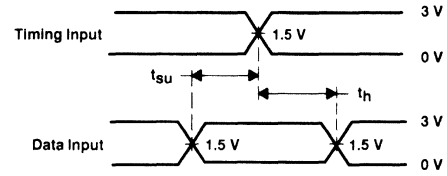


LOAD CIRCUIT FOR A OUTPUTS

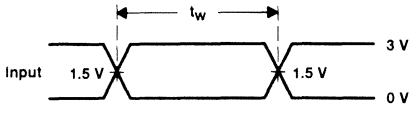


LOAD CIRCUIT FOR B OUTPUTS

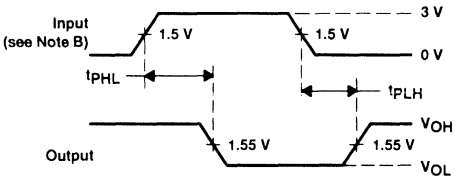
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



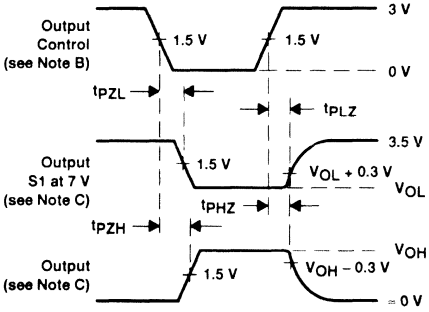
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



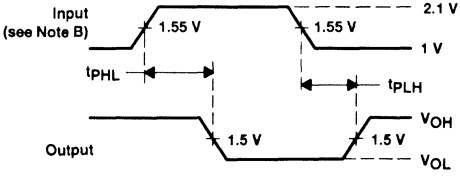
VOLTAGE WAVEFORMS
PULSE DURATION



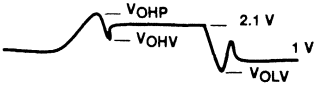
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (A to B)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES (A port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (B to A)



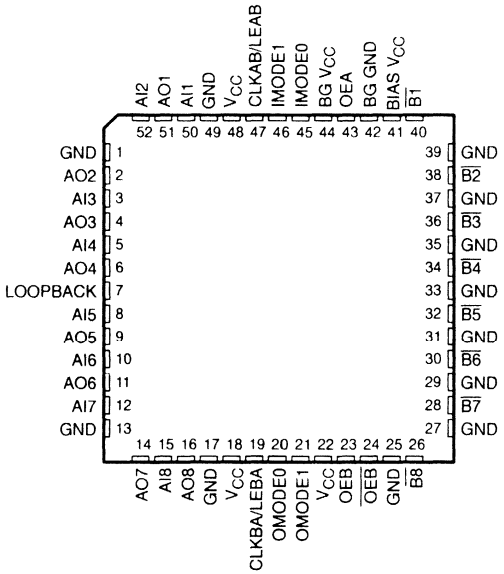
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: TTL inputs – PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns, BTL inputs – PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuits and Voltage Waveforms

- TTL A Port, Backplane Transceiver Logic (BTL) $\overline{B}$ Port
- Open-Collector $\overline{B}$-Port Outputs Sink 100 mA
- Isolated Logic-Ground and Bus-Ground Pins Reduce Noise
- BIAS V_{CC} Pin Minimizes Signal Distortion During Live Insertion/Withdrawal
- $\overline{B}$-Port Biasing Network Preconditions the Connector and PC Trace to the Backplane Transceiver Logic High-Level Voltage
- TTL-Input Structures Incorporate Active Clamping Networks to Aid in Line Termination
- Available in Plastic Quad Flatpack (RC) Package

RC PACKAGE
(TOP VIEW)



description

The SN74FB2033H is an 8-bit transceiver featuring a split input (AI) and output (AO) bus on the TTL-level A port. The common I/O, open-collector $\overline{B}$ port operates at backplane transceiver logic (BTL) signal levels.

The logic element for data flow in each direction is configured by two mode inputs (IMODE1 and IMODE0 for B-to-A, OMODE1 and OMODE0 for A-to-B) as a buffer, a D-type flip-flop, or a D-type latch. When configured in the buffer mode, the inverted input data appears at the output port. In the flip-flop mode, data is stored on the rising edge of the appropriate clock input (CLKAB/LEAB or CLKBA/LEBA). In the latch mode, the clock pins serve as active-high transparent latch enables.

Data flow in the B-to-A direction, regardless of the logic element selected, is further controlled by the LOOPBACK input. When LOOPBACK is low, $\overline{B}$-port data is the B-to-A input. When LOOPBACK is high, the output of the selected A-to-B logic element (prior to inversion) is the B-to-A input.

description (continued)

The AO port-enable/-disable control is provided by OEA. When OEA is low or when V_{CC} is less than 2.5 V, the AO port is in the high-impedance state. When OEA is high, the AO port is active (high or low logic levels).

The $\overline{B}$ port is controlled by OEB and $\overline{OEB}$. If OEB is low, or $\overline{OEB}$ is high, or when V_{CC} is less than 2.5 V, the $\overline{B}$ port is inactive. If OEB is high and $\overline{OEB}$ is low, the B port is active.

BG V_{CC} and BG GND are the bias-generator reference inputs.

The A-to-B and B-to-A logic elements are active regardless of the state of their associated outputs. The logic elements can enter new data (in flip-flop and latch modes) or retain previously stored data while the associated outputs are in the high-impedance (AO port) or inactive ($\overline{B}$ port) states.

Output clamps are provided on the BTL outputs to reduce switching noise. One clamp reduces inductive ringing effects on V_{OH} during a low-to-high transition. The other clamps out ringing below the BTL V_{OL} voltage of 0.75 V. Both these clamps are active only during AC switching and do not affect the BTL outputs during steady-state conditions.

BIAS V_{CC} establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when V_{CC} is not connected.

The SN74FB2033H is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS								FUNCTION/MODE
OEA	OEB	$\overline{OEB}$	OMODE1	OMODE0	IMODE1	IMODE0	LOOPBACK	
L	L	X	X	X	X	X	X	Isolation
L	X	H	X	X	X	X	X	
X	H	L	L	L	X	X	X	AI to $\overline{B}$, buffer mode
X	H	L	L	H	X	X	X	AI to $\overline{B}$, flip-flop mode
X	H	L	H	X	X	X	X	AI to $\overline{B}$, latch mode
H	L	X	X	X	L	L	L	$\overline{B}$ to AO, buffer mode
H	X	H	X	X	L	L	L	
H	L	X	X	X	L	H	L	$\overline{B}$ to AO, flip-flop mode
H	X	H	X	X	L	H	L	
H	L	X	X	X	H	X	L	$\overline{B}$ to AO, latch mode
H	X	H	X	X	H	X	L	
H	L	X	X	X	L	L	H	AI to AO, buffer mode
H	X	H	X	X	L	L	H	
H	L	X	X	X	L	H	H	AI to AO, flip-flop mode
H	X	H	X	X	L	H	H	
H	L	X	X	X	H	X	H	AI to AO, latch mode
H	X	H	X	X	H	X	H	
H	H	L	X	X	X	X	L	AI to $\overline{B}$, $\overline{B}$ to AO

Function Tables

ENABLE/DISABLE

INPUTS			OUTPUTS	
OEA	OEB	$\overline{OEB}$	AO	$\overline{B}$
L	X	X	Hi Z	
H	X	X	Active	
X	L	L		Inactive (H)
X	L	H		Inactive (H)
X	H	L		Active
X	H	H		Inactive (H)

BUFFER

INPUT	OUTPUT
L	H
H	L

LATCH

INPUTS		OUTPUT
CLK/LE	DATA	
H	L	H
H	H	L
L	X	Q_0

LOOPBACK

LOOPBACK	Q†
L	$\overline{B}$ port
H	Point P‡

† Q is the input to the B-to-A logic element.

‡ P is the output of the A-to-B logic element (see functional block diagram).

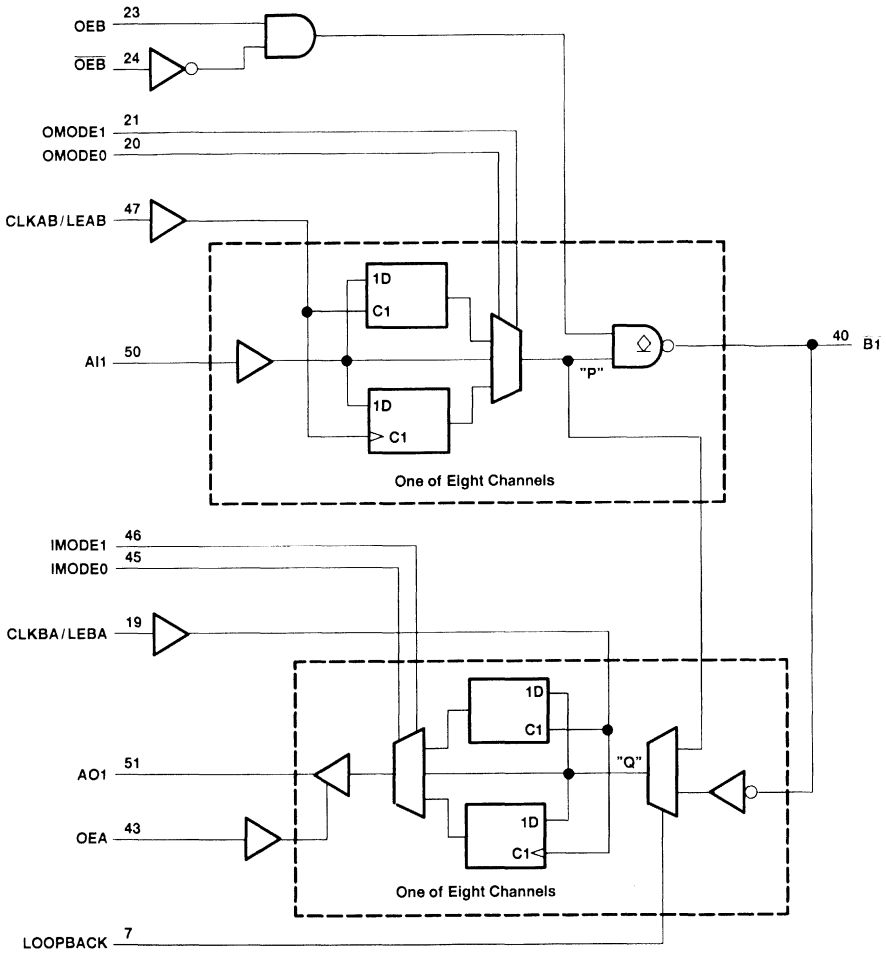
SELECT

INPUTS		SELECTED-LOGIC ELEMENT
MODE1	MODE0	
L	L	Buffer
L	H	Flip-flop
H	X	Latch

FLIP-FLOP

INPUTS		OUTPUT
CLK/LE	DATA	
L	X	Q_0
↑	L	H
↑	H	L

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I: except $\overline{B}$ port ..... −1.2 V to 7 V
$\overline{B}$ port ..... −1.2 V to 3.5 V
Input current range (except $\overline{B}$ port) ..... −40 mA to 5 mA
Voltage range applied to any B output in the disabled or power-off state ..... −0.5 V to 3.5 V
Voltage range applied to any output in the high state: A port ..... −0.5 V to V_{CC}
Current applied to any single output in the low state: A port ..... 48 mA
$\overline{B}$ port ..... 200 mA
Maximum power dissipation at T_A = 55°C (in still air) ..... 1.4 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 1)

			MIN	NOM	MAX	UNIT
V_{CC}, BG V_{CC}	Supply voltage		4.75	5	5.25	V
BIAS V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage	$\overline{B}$ port	1.62		2.3	V
		Except $\overline{B}$ port	2			
V_{IL}	Low-level input voltage	$\overline{B}$ port	0.75		1.47	V
		Except $\overline{B}$ port			0.8	
I_{OH}	High-level output current	AO port			−3	mA
I_{OL}	Low-level output current	AO port			24	mA
		$\overline{B}$ port			100	
$\Delta t/\Delta v$	Input transition rise or fall rate	Except $\overline{B}$ port			10	ns/V
T_A	Operating free-air temperature		0		70	°C

NOTE 1: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V,	I_I = −18 mA			−1.2	V
V_{OH}	AO port	V_{CC} = 4.75 V to 5.25 V,	I_{OH} = −10 μA			V_{CC}−1.1	V
		V_{CC} = 4.75 V	I_{OH} = −3 mA	2.5	2.85	3.4	
			I_{OH} = −32 mA	2			
V_{OL}	AO port	V_{CC} = 4.75 V	I_{OL} = 20 mA		0.33	0.5	V
			I_{OL} = 55 mA			0.8	
	$\overline{B}$ port	V_{CC} = 4.75 V	I_{OL} = 100 mA	0.75		1.1	
			I_{OL} = 4 mA	0.5			
I_I	Except $\overline{B}$ port	V_{CC} = 0,	V_I = 5.25 V			100	μA
I_{IH}	Except $\overline{B}$ port	V_{CC} = 5.25 V,	V_I = 2.7 V			50	μA
	$\overline{B}$ port‡	V_{CC} = 0 to 5.25 V,	V_I = 2.1 V			100	
I_{IL}	Except $\overline{B}$ port	V_{CC} = 5.25 V,	V_I = 0.5 V			−50	μA
	$\overline{B}$ port‡	V_{CC} = 5.25 V,	V_I = 0.75 V			−100	
I_{OH}	$\overline{B}$ port	V_{CC} = 0 to 5.25 V,	V_O = 2.1 V			100	μA
I_{OZH}	AO port	V_{CC} = 5.25 V,	V_O = 2.7 V			50	μA
I_{OZL}	AO port	V_{CC} = 5.25 V,	V_O = 0.5 V			−50	μA
I_{OS}§	AO port	V_{CC} = 5.25 V,	V_O = 0	−40	−80	−150	mA
I_{CC}	All outputs on	V_{CC} = 5.25 V,	I_O = 0		45	70	mA
C_i	AI port and control inputs	V_I = V_{CC} or GND			5		pF
C_o	AO port	V_O = V_{CC} or GND			5		pF
C_{io}¶	$\overline{B}$ port per P1194.0	V_{CC} = 0 to 4.75 V				6	pF
		V_{CC} = 4.75 V to 5.25 V				6	

† All typical values are at V_{CC} = 5 V.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
¶ Parameter is based on characterization data but is not tested.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)

		V_{CC} = 5 V, T_A = 25°C		MIN	MAX	UNIT
		MIN	MAX			
f_{clock}	Clock frequency	0	150	0	150	MHz
t_w	Pulse duration, CLKAB/LEAB or CLKBA/LEBA	3.3		3.3		ns
t_{su}	Setup time, data before CLKAB/LEAB or CLKBA/LEBA↑	2.7		2.7		ns
t_h	Hold time, data after CLKAB/LEAB or CLKBA/LEBA↑	0.7		0.7		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			150			150		MHz
t_{PLH}	AI (thru mode)	$\overline{B}$	2.8	5.1	6.8	2.8	8.1	ns
t_{PHL}			2.5	4.2	5.7	2.5	6.1	
t_{PLH}	B (thru mode)	AO	2.2	4.3	6	2.2	6.6	ns
t_{PHL}			2.6	4.2	5.6	2.6	6	
t_{PLH}	AI (transparent)	$\overline{B}$	2.8	5.1	6.8	2.8	8.1	ns
t_{PHL}			2.6	4.2	5.7	2.6	6.1	
t_{PLH}	B (transparent)	AO	2.2	4.3	6	2.2	6.6	ns
t_{PHL}			2.5	4.2	5.6	2.5	6	
t_{PLH}	OEB	$\overline{B}$	2.7	5.1	6.8	2.7	8.3	ns
t_{PHL}			2.4	4.2	5.7	2.4	6.1	
t_{PLH}	OEB	$\overline{B}$	2.5	4.8	6.4	2.5	7.7	ns
t_{PHL}			2.5	4.3	5.9	2.5	6.4	
t_{PZH}	OEA	AO	1.6	3.6	5.1	1.6	5.6	ns
t_{PZL}			2.3	4.3	5.7	2.3	6	
t_{PHZ}	OEA	AO	1.7	4	5.5	1.7	5.9	ns
t_{PLZ}			1.2	2.9	4.4	1.2	4.7	
t_{PLH}	CLKAB/LEAB	$\overline{B}$	3.7	6.5	8.3	3.7	9.9	ns
t_{PHL}			3.4	5.4	7.1	3.4	7.7	
t_{PLH}	CLKBA/LEBA	AO	4.7	3.8	5.5	4.7	5.9	ns
t_{PHL}			4.8	3.6	5.1	4.8	5.5	
t_{PLH}	OMODE	$\overline{B}$	2.9	6.6	8.4	2.9	10	ns
t_{PHL}			3	5.7	7.5	3	8.3	
t_{PLH}	IMODE	AO	1.4	4.1	5.8	1.4	6.4	ns
t_{PHL}			1.9	4.2	5.7	1.9	5.9	
t_{PLH}	LOOPBACK	AO	2	5.2	7.3	2	8.2	ns
t_{PHL}			2.6	4.8	6.3	2.6	6.4	
t_{PLH}	AI	AO	1.7	3.9	5.6	1.7	6.1	ns
t_{PHL}			2.2	4.3	5.7	2.2	5.9	
t_t	Rise time, 1.3 V to 1.8 V	$\overline{B}$	1.8	2.5	3.8	1.7	4	ns
	Fall time, 1.8 V to 1.3 V		1.7	2.5	3.8	1.5	4	
	Rise time, 10% to 90%	AO	2.5	3.4	4.8	2	5	
	Fall time, 90% to 10%		1.5	2.5	3.8	1	5	
t_{PR}	B-port input pulse rejection					1		ns

live-insertion characteristics over recommended operating free-air temperature range (see Note 2)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
I_{CC} (BIAS V_{CC})		V_{CC} = 0 to 4.5 V	V_B = 0 to 2 V, BIAS V_{CC} = 4.5 V to 5.5 V		400	μA
		V_{CC} = 4.5 V to 5.5 V			10	
V_O	$\overline{B}$ port	V_{CC} = 0,	BIAS V_{CC} = 4.5 V to 5.5 V	1.62	2.1	V
I_O	B port	V_{CC} = 0, V_I (BIAS V_{CC}) = 4.5 V to 5.5 V	V_B = 1 V,	−1		μA
		V_{CC} = 0 to 5.5 V,	OEB = 0 to 0.8 V		100	
		V_{CC} = 0 to 2.2 V,	OEB = 0 to 5 V		100	

NOTE 2: Power-up sequence is as follows: GND, BIASV_{CC}, V_{CC}.

switching characteristics (see Figure 2)

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OHP}†	Peak output voltage during turnoff of 100 mA into 40 nH	$\overline{B}$ port	See Figure 1		3	V
V_{OHV}†	Minimum output voltage during turnoff of 100 mA into 40 nH	$\overline{B}$ port	See Figure 1	1.62		V
V_{OLV}	Minimum output voltage during high-to-low switch	$\overline{B}$ port	I_{OL} = −50 mA	0.3		V

† Parameter is based on characterization data but not tested.

PARAMETER MEASUREMENT INFORMATION

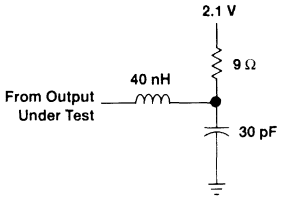
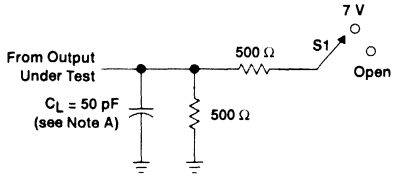
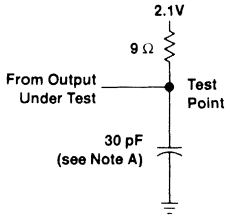


Figure 1. Load Circuit for V_{OHP}, V_{OHV}

PARAMETER MEASUREMENT INFORMATION

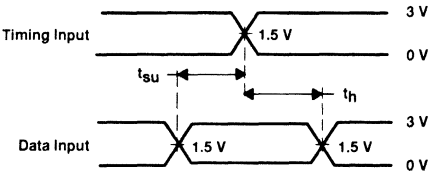


LOAD CIRCUIT FOR A OUTPUTS

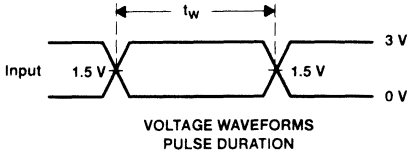


LOAD CIRCUIT FOR B OUTPUTS

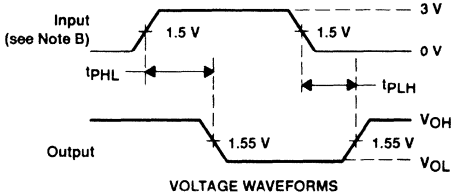
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



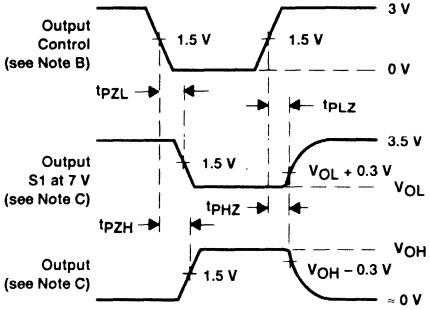
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



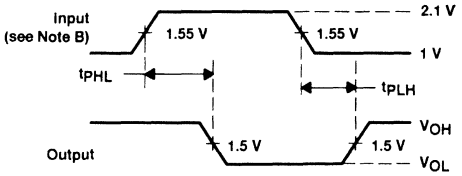
VOLTAGE WAVEFORMS
PULSE DURATION



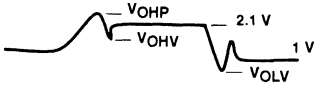
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (A TO B)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES (A PORT)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (B TO A)



VOLTAGE WAVEFORMS

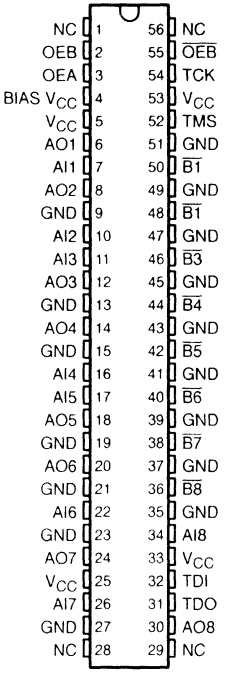
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: TTL inputs - PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns, BTL inputs - PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

SCBS173B – NOVEMBER 1991 – REVISED SEPTEMBER 1994

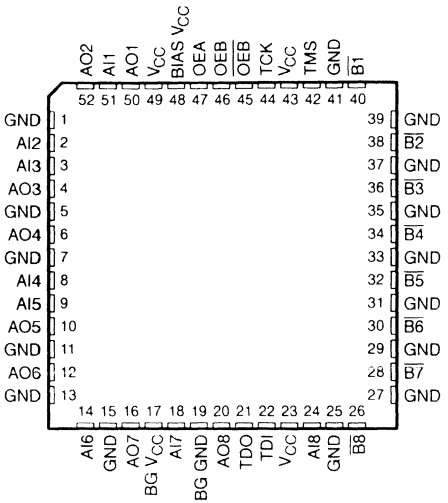
- **Compatible With IEEE 1194.1-1991 (BTL) Standard**
- **TTL A Port, Backplane Transceiver Logic $\overline{B}$ Port**
- **Open-Collector $\overline{B}$-Port Outputs Sink 100 mA**
- **Isolated Logic-Ground and Bus-Ground Reduces Noise**
- **BIAS V_{CC} Pin Minimizes Signal Distortion During Live Insertion/Withdrawal**
- **$\overline{B}$-Port Biasing Network Preconditions the Connector and PC Trace to the Backplane Transceiver Logic High-Level Voltage**
- **Package Options Include Plastic Quad Flat (RC) Package and Ceramic Flat (WD) Package**

SN54FB2040 . . . WD PACKAGE
(TOP VIEW)



NC – No internal connection

SN74FB2040 . . . RC PACKAGE
(TOP VIEW)



description

The 'FB2040 are 8-bit transceivers designed to translate signals between TTL and backplane transceiver logic (BTL) environments.

The $\overline{B}$ port operates at BTL-signal levels. The open-collector $\overline{B}$ ports are specified to sink 100 mA. Two output enables, OEB and $\overline{OEB}$, are provided for the $\overline{B}$ outputs. When OEB is high and $\overline{OEB}$ is low, the $\overline{B}$ port is active and reflects the inverse of the data present at the A-input pins. When OEB is low, $\overline{OEB}$ is high, or V_{CC} is typically less than 2.5 V, the $\overline{B}$ port is turned off.

description (continued)

The A port operates at TTL-signal levels and has split input and output pins. The A outputs reflect the inverse of the data at the $\overline{B}$ port when the A-port output enable, OEA, is high. When OEA is low or when V_{CC} is typically less than 2.5 V, the A outputs are in the high-impedance state.

Pins are allocated for the four-wire IEEE 1149.1 (JTAG) test bus. Currently, TMS and TCK are not connected and TDI is shorted to TDO.

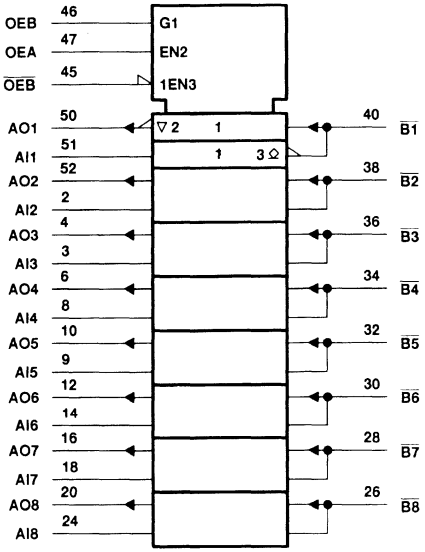
BIAS V_{CC} establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when V_{CC} is not connected.

The SN54FB2040 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74FB2040 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

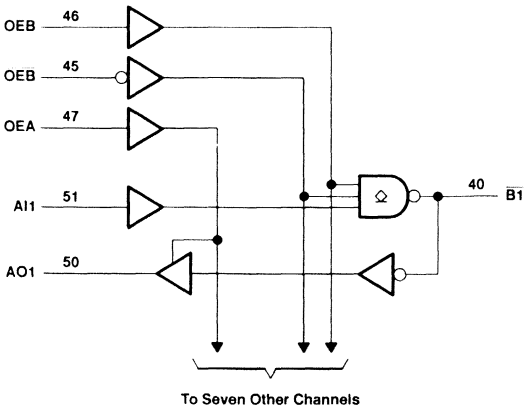
INPUTS			FUNCTION
OEB	$\overline{OEB}$	OEA	
L	X	L	Isolation
X	H	L	
L	X	H	$\overline{B}$ data to AO bus
X	H	H	
H	L	L	$\overline{AI}$ data to B bus
H	L	H	$\overline{AI}$ data to B bus, $\overline{B}$ data to AO bus

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the RC package.

functional block diagram



Pin numbers shown are for the RC package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I: except $\overline{B}$ port ..... −1.2 V to 7 V
$\overline{B}$ port ..... −1.2 V to 3.5 V
Input current range (except $\overline{B}$ port) ..... −40 mA to 5 mA
Voltage range applied to any $\overline{B}$ output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage range applied to any output in the high state ..... −0.5 V to V_{CC}
Current applied to any single output in the low state: A port ..... 48 mA
$\overline{B}$ port ..... 200 mA
Operating free-air temperature range, T_A: SN54FB2040 ..... −55°C to 125°C
SN74FB2040 ..... 0°C to 70°C
Maximum power dissipation at T_A = 55°C (in still air) (see Note 1): RC package ..... 1.4 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 75 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 2)

			SN54FB2040			SN74FB2040			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}, BIAS V_{CC}, BG V_{CC}	Supply voltage		4.75	5	5.25	4.5	5	5.5	V
V_{IH}	High-level input voltage	$\overline{B}$ port*	1.62		2.3	1.62		2.3	V
		Except $\overline{B}$ port	2			2			
V_{IL}	Low-level input voltage	$\overline{B}$ port*	0.75		1.47	0.75		1.47	V
		Except $\overline{B}$ port			0.8			0.8	
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	High-level output current	AO port						−3	mA
I_{OL}	Low-level output current	AO port						24	mA
		$\overline{B}$ port			100			100	
T_A	Operating free-air temperature		−55		125	0		70	°C

* On products compliant to MIL-STD-833, Class B, this parameter is based on characterization data but is not tested.
NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54FB2040			SN74FB2040			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$\overline{B}$ port	V_{CC} = 4.5 V	I_I = −18 mA			−1.2			−1.2	V
	Except $\overline{B}$ port		I_I = −40 mA			−1.2			−0.5	
V_{OH}	AO port	V_{CC} = 4.5 V	I_{OH} = −1 mA		3.2					V
			I_{OH} = −3 mA	2.5	3.3		2.5	3.3		
V_{OL}	AO port	V_{CC} = 4.5 V	I_{OL} = 20 mA		0.09					V
			I_{OL} = 24 mA		0.35	0.5		0.35	0.5	
	$\overline{B}$ port	V_{CC} = 4.5 V	I_{OL} = 80 mA	0.75		1.1	0.75		1.1	
			I_{OL} = 100 mA			1.2			1.15	
I_I	Except $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 5.5 V			50			50	µA
I_{IH}‡	Except $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 2.7 V			50			50	µA
I_{IL}‡	Except $\overline{B}$ port	V_{CC} = 5.5 V	V_I = 0.5 V			−50			−50	µA
	$\overline{B}$ port		V_I = 0.75 V			−100			−100	
I_{OH}	$\overline{B}$ port	V_{CC} = 0 to 5.5 V,	V_O = 2.1 V			100			100	µA
I_{OZH}	AO port	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	µA
I_{OZL}	AO port	V_{CC} = 5.5 V,	V_O = 0.5 V			−50			−50	µA
I_{OS}§	AO port	V_{CC} = 5.5 V,	V_O = 0	−30		−170	−30		−180	mA
I_{CC}	AI port to $\overline{B}$ port	V_{CC} = 5.5 V,	I_O = 0		25	40		40		mA
	$\overline{B}$ port to AO port				60	70		70		
C_i	AI port*	V_I = V_{CC} or GND			25	70		3.5		pF
	Control inputs*					9.9		3		
C_o	AO port*	V_O = V_{CC} or GND				14.7		6		pF
C_{io}	$\overline{B}$ port per P1194.0*	V_{CC} = 0 to 4.5 V				8			5	pF
		V_{CC} = 4.5 V to 5.5 V				9			5	

* On products compliant to MIL-STD-833, Class B, this parameter is based on characterization data but is not tested.
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

live-insertion specifications over recommended operating free-air temperature range

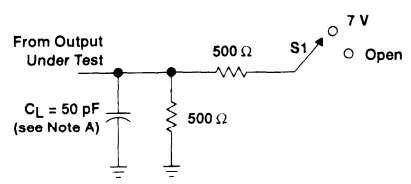
PARAMETER		TEST CONDITIONS		SN54FB2040		SN74FB2040		UNIT
				MIN	MAX	MIN	MAX	
I_{CC} (BIAS V_{CC})		V_{CC} = 0 to 4.5 V	V_B = 0 to 2 V, V_I (BIAS V_{CC}) = 4.5 V to 5.5 V		450		450	μA
		V_{CC} = 4.5 to 5.5 V			10		10	
V_O	$\overline{B}$ port	V_{CC} = 0,	V_I (BIAS V_{CC}) = 4.5 V to 5.5 V	1.62	2.1	1.62	2.1	V
I_O	$\overline{B}$ port	V_{CC} = 0,	V_B = 1 V, V_I (BIAS V_{CC}) = 4.5 V to 5.5 V	−30		−1		μA
		V_{CC} = 0 to 5.5 V,	OEB = 0 to 0.8 V		100		100	
		V_{CC} = 0 to 2.2 V,	OEB = 0 to 5 V		100		100	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

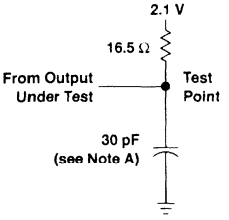
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54FB2040		SN74FB2040		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	AI	$\overline{B}$	3.2	4.5	6	0.5	8.5	2.4	6.5	ns
t_{PHL}			2.8	4.2	5.6	0.4	8.5	2.7	5.8	
t_{PLH}	$\overline{B}$	AO	2.3	3.8	5.7	0.4	8	1.9	6.2	ns
t_{PHL}			2.3	4.2	5.9	0.8	14.9	2	8.2	
t_{PLH}	OEB	$\overline{B}$	3.7	5.1	6.7	0.5	9.9	3	7	ns
t_{PHL}			3.1	4.6	5.9	0.4	9.5	3	6.1	
t_{PLH}	$\overline{OEB}$	$\overline{B}$	3.6	5.2	6.8	1.3	9.5	3.3	7	ns
t_{PHL}			2.9	4.4	5.9	0.2	9.8	2.6	6.1	
t_{PZH}	OEA	AO	2.5	4	5.5	1.2	8	2.1	5.8	ns
t_{PZL}			2.1	3.6	4.8	0.8	7.5	2	5	
t_{PHZ}	OEA	AO	2.3	4.1	5.9	1	8.2	1.9	6.5	ns
t_{PLZ}			1.6	3.1	4.5	0.4	7.2	1.4	4.7	
$t_{sk(p)}$*	Skew for any single channel $\lvert t_{PHL} - t_{PLH} \rvert$	AI to $\overline{B}$ or $\overline{B}$ to AO		0.5						ns
$t_{sk(o)}$*	Skew between drivers in the same package	AI to B or B to AO		0.4			2			ns
t_t	Rise time, 1.3 V to 1.8 V	$\overline{B}$	2	2.8	3.8	0.2	4.5	1.7		
	Fall time, 1.8 V to 1.3 V		1	1.9	3	0.9	4.0	1	4.2	
t_{PR}*	$\overline{B}$-port input pulse rejection							1	3.4	ns

* On products compliant to MIL-STD-833, Class B, this parameter is based on characterization data but is not tested.

PARAMETER MEASUREMENT INFORMATION

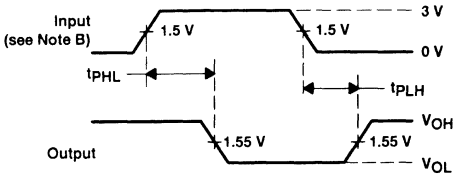


LOAD CIRCUIT FOR A OUTPUTS

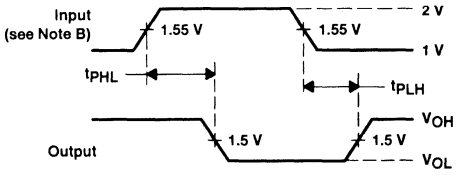


LOAD CIRCUIT FOR B OUTPUTS

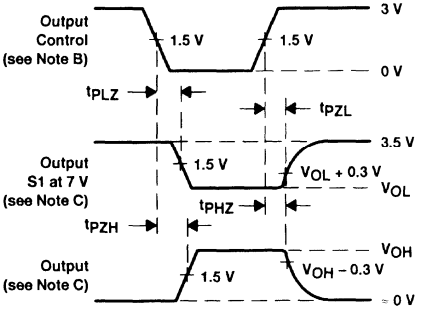
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (A to B)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (B to A)



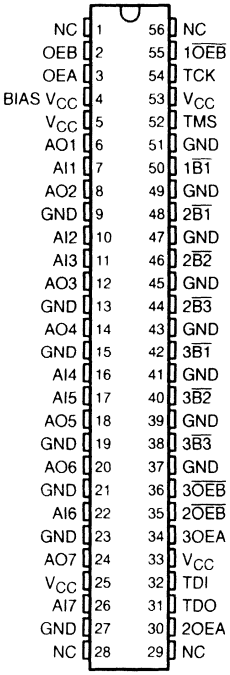
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES (A port)

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: TTL inputs – PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns. BTL inputs – PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

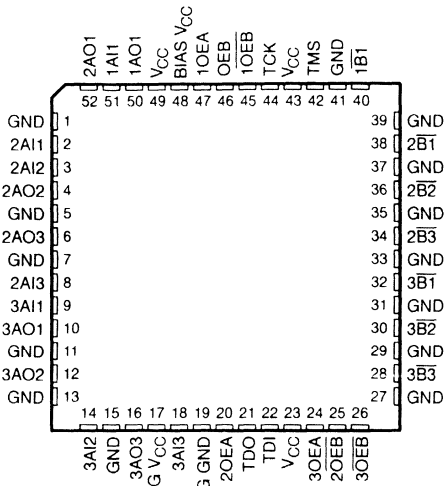
- **Compatible With IEEE 1194.1-1991 (BTL) Standard**
- **TTL A Port, Backplane Transceiver Logic $\overline{B}$ Port**
- **Open-Collector $\overline{B}$-Port Outputs Sink 100 mA**
- **Isolated Logic-Ground and Bus-Ground Reduces Noise**
- **BIAS V_{CC} Pin Minimizes Signal Distortion During Live Insertion/Withdrawal**
- **$\overline{B}$-Port Biasing Network Preconditions the Connector and PC Trace to the Backplane Transceiver Logic High-Level Voltage**
- **Package Options Include Plastic Quad Flat (RC) Package and Ceramic Flat (WD) Package**

SN54FB2041 . . . WD PACKAGE
(TOP VIEW)



NC – No internal connection

SN74FB2041 . . . RC PACKAGE
(TOP VIEW)



description

The 'FB2041 are 7-bit transceivers designed to translate signals between TTL and backplane transceiver logic (BTL) environments.

The $\overline{B}$ port operates at BTL-signal levels. The open-collector $\overline{B}$ ports are specified to sink 100 mA. Two output enables, OEB and $\overline{OEB}$, are provided for the $\overline{B}$ outputs. When OEB is high and $\overline{OEB}$ is low, the $\overline{B}$ port is active and reflects the inverse of the data present at the A-input pins. When OEB is low, $\overline{OEB}$ is high, or V_{CC} is typically less than 2.5 V, the $\overline{B}$ port is turned off. The enable/disable logic partitions the device as two 3-bit sections and one 1-bit section.

description (continued)

The A port operates at TTL-signal levels and has split input and output pins. The A outputs reflect the inverse of the data at the $\overline{B}$ port when the A-port output enable, OEA, is high. When OEA is low or when V_{CC} is typically less than 2.5 V, the A outputs are in the high-impedance state.

Pins are allocated for the four-wire IEEE 1149.1 (JTAG) test bus. Currently, TMS and TCK are not connected and TDI is shorted to TDO.

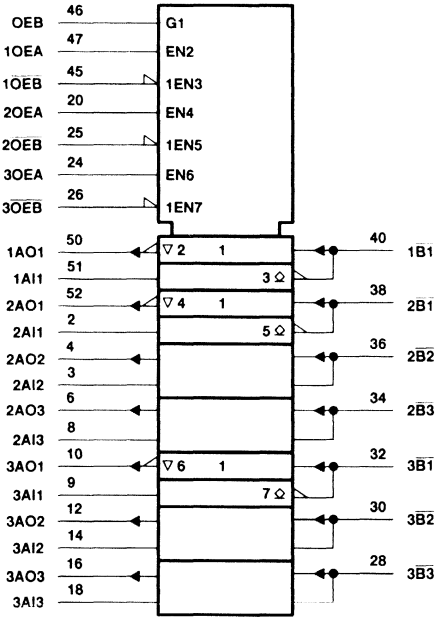
BIAS V_{CC} establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when V_{CC} is not connected.

The SN54FB2041 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74FB2041 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

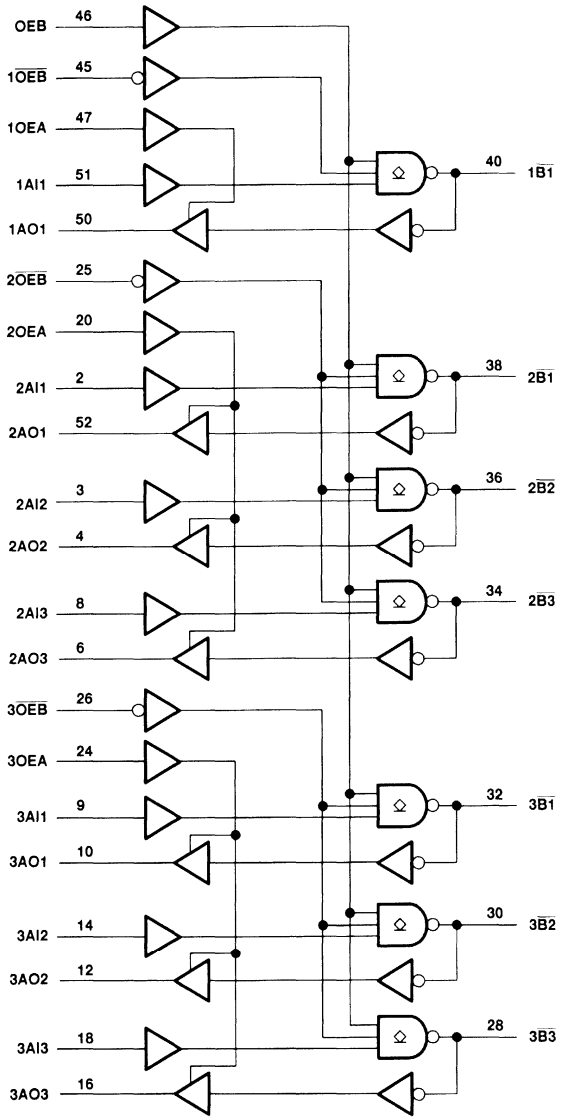
INPUTS			FUNCTION
OEB	$\overline{OEB}$	OEA	
L	X	L	Isolation
X	H	L	
L	X	H	$\overline{B}$ data to AO bus
X	H	H	
H	L	L	$\overline{AI}$ data to B bus
H	L	H	$\overline{AI}$ data to B bus, $\overline{B}$ data to AO bus

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the RC package.

functional block diagram



Pin numbers shown are for the RC package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I: except $\overline{B}$ port ..... −1.2 V to 7 V
$\overline{B}$ port ..... −1.2 V to 3.5 V
Input current range (except $\overline{B}$ port) ..... −40 mA to 5 mA
Voltage range applied to any $\overline{B}$ output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage range applied to any output in the high state ..... −0.5 V to V_{CC}
Current applied to any single output in the low state: A port ..... 48 mA
$\overline{B}$ port ..... 200 mA
Operating free-air temperature range, T_A: SN54FB2041 ..... −55°C to 125°C
SN74FB2041 ..... 0°C to 70°C
Maximum power dissipation at T_A = 55°C (in still air) (see Note 1): RC package ..... 1.4 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 75 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 2)

			SN54FB2041			SN74FB2041			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}, BIAS V_{CC}, BG V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	$\overline{B}$ port	1.62		2.3	1.62		2.3	V
		Except $\overline{B}$ port	2			2			
V_{IL}	Low-level input voltage	$\overline{B}$ port	0.75		1.47	0.75		1.47	V
		Except $\overline{B}$ port			0.8			0.8	
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	High-level output current	AO port			−3			−3	mA
I_{OL}	Low-level output current	AO port			24			24	mA
		B port			100			100	
T_A	Operating free-air temperature		−55		125	0		70	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54FB2041			SN74FB2041			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$\overline{B}$ port	V_{CC} = 4.5 V	I_I = −18 mA			−1.2			−1.2	V
	Except $\overline{B}$ port		I_I = −40 mA			−0.5			−0.5	
V_{OH}	AO port	V_{CC} = 4.5 V	I_{OH} = −1 mA							V
			I_{OH} = −3 mA	2.5	3.3		2.5	3.3		
V_{OL}	AO port	V_{CC} = 4.5 V	I_{OL} = 20 mA							V
			I_{OL} = 24 mA		0.35	0.5		0.35	0.5	
	$\overline{B}$ port	V_{CC} = 4.5 V	I_{OL} = 80 mA	0.75		1.1	0.75		1.1	
			I_{OL} = 100 mA			1.15			1.15	
I_I	Except $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 5.5 V			50			50	µA
I_{IH}‡	Except $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 2.7 V			50			50	µA
I_{IL}‡	Except $\overline{B}$ port	V_{CC} = 5.5 V	V_I = 0.5 V			−50			−50	µA
	$\overline{B}$ port		V_I = 0.75 V			−100			−100	
I_{OH}	$\overline{B}$ port	V_{CC} = 0 to 5.5 V,	V_O = 2.1 V			100			100	µA
I_{OZH}	AO port	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	µA
I_{OZL}	AO port	V_{CC} = 5.5 V,	V_O = 0.5 V			−50			−50	µA
I_{OS}§	AO port	V_{CC} = 5.5 V,	V_O = 0	−30		−150	−30		−180	mA
I_{CC}	AI port to $\overline{B}$ port	V_{CC} = 5.5 V,	I_O = 0		25			40		mA
	$\overline{B}$ port to AO port				65			65		
C_i	AI port	V_I = V_{CC} or GND						3.5		pF
	Control inputs							3		
C_o	AO port	V_O = V_{CC} or GND						6		pF
C_{io}	$\overline{B}$ port per P1194.0	V_{CC} = 0 to 4.5 V				6			5	pF
		V_{CC} = 4.5 V to 5.5 V				5			5	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

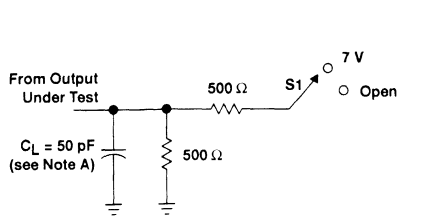
live-insertion specifications over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		SN54FB2041		SN74FB2041		UNIT
				MIN	MAX	MIN	MAX	
I_{CC} (BIAS V_{CC})		V_{CC} = 0 to 4.5 V	V_B = 0 to 2 V, V_I (BIAS V_{CC}) = 4.5 V to 5.5 V		450		450	µA
		V_{CC} = 4.5 V to 5.5 V			10		10	
V_O	$\overline{B}$ port	V_{CC} = 0,	V_I (BIAS V_{CC}) = 4.5 V to 5.5 V	1.62	2.1	1.62	2.1	V
I_O	$\overline{B}$ port	V_{CC} = 0, V_I (BIAS V_{CC}) = 4.5 V to 5.5 V	V_B = 1 V,	−1		−1		µA
		V_{CC} = 0 to 5.5 V,	OEB = 0 to 0.8 V		100		100	
		V_{CC} = 0 to 2.2 V,	OEB = 0 to 5 V		100		100	

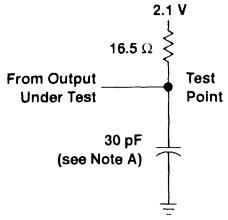
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54FB2041		SN74FB2041		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	AI	$\overline{B}$	3	4.6	6			2.7	6.5	ns
t_{PHL}			2.7	4.2	5.6			2.5	5.8	
t_{PLH}	B	AO	2.2	3.7	5.5			1.8	6	ns
t_{PHL}			2.6	4.1	5.9			2.2	7.9	
t_{PLH}	OEB	$\overline{B}$	3.8	5.3	7.1			3.3	7.4	ns
t_{PHL}			3.4	4.9	6.5			3.2	6.7	
t_{PLH}	OEB	B	3.7	5.1	6.8			3.4	7	ns
t_{PHL}			2.9	4.4	6.2			2.4	6.4	
t_{PZH}	OEA	AO	1.8	3.3	5.1			1.5	5.6	ns
t_{PZL}			1.7	3.1	4.7			1.6	5	
t_{PHZ}	OEA	AO	1.9	3.3	5			1.3	5.3	ns
t_{PLZ}			1.1	2.6	4.3			0.9	4.7	
$t_{sk(p)}$	Skew for any single channel $\lvert t_{PHL} - t_{PLH} \rvert$	AI to $\overline{B}$ or $\overline{B}$ to AO		0.5						ns
$t_{sk(o)}$	Skew between drivers in the same package	AI to $\overline{B}$ or $\overline{B}$ to AO		0.4						ns
t_t	Rise time, 1.3 V to 1.8 V	$\overline{B}$	2.4	3.5	4.6			2.2	5.2	
	Fall time, 1.8 V to 1.3 V		1	2	3			1	3.4	
t_{PR}	$\overline{B}$-port input pulse rejection					1		1		ns

PARAMETER MEASUREMENT INFORMATION

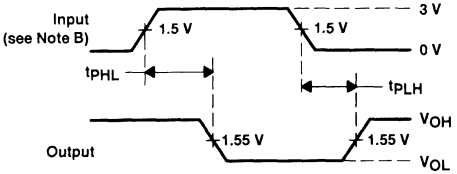


LOAD CIRCUIT FOR A OUTPUTS

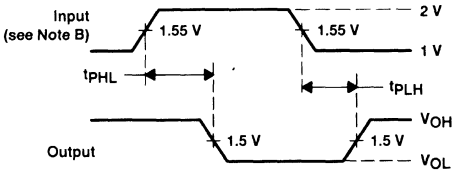


LOAD CIRCUIT FOR B OUTPUTS

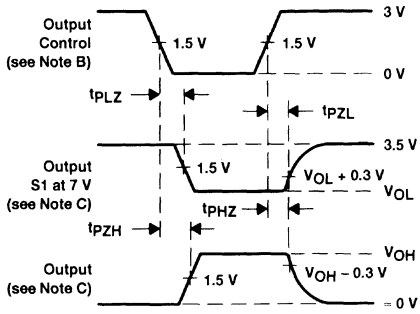
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (A to B)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (B to A)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES (A port)

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: TTL inputs – PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns. BTL inputs – PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

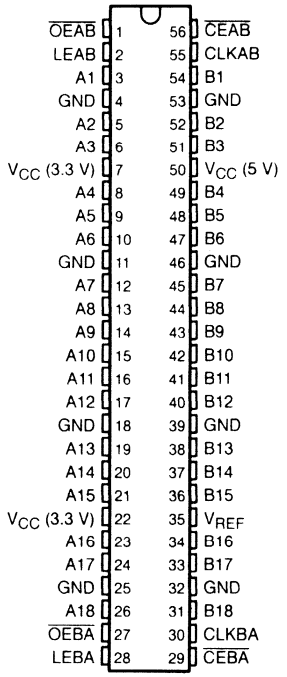
Figure 1. Load Circuits and Voltage Waveforms

The new TI Gunning Transceiver Logic (GTL) family allows designers of high-performance workstation and networking equipment to achieve higher speeds with much less power-consumption overhead. GTL transceivers use a 0.8 V output switching region with a very small (100 mV) input threshold, to handle device speeds as high as 150 MHz. Applications are GTL backplanes that require TTL translation, memory array point-to-point drivers, and local-bus interface drivers between a GTL processing system and a TTL bus.

SCBS480B – JUNE 1994 – REVISED OCTOBER 1994

- **Translates Between GTL Logic Levels and LVTTL or 5-V TTL Logic Levels**
- **Members of the Texas Instruments *Widebus*™ Family**
- **Support Mixed-Mode Signal Operation on A Port**
- **Universal Bus Transceiver (*UBT*™) Combines D-Type Latches and D-Type Flip-Flops With Qualified Storage Enable**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors on A Port**
- **Flow-Through Architecture Optimizes Printed-Circuit-Board Layout**
- **Package Options Include Plastic Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Ceramic Flat (WD) Packages**

SN54GTL16612 . . . WD PACKAGE
SN74GTL16612 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

These 18-bit bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

The B port operates at GTL levels while the A port and control pins are compatible with LVTTL or 5-V TTL logic levels.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock or latch-enable can be controlled by the clock-enable ($\overline{CEAB}$ and $\overline{CEBA}$) inputs. For A-to-B data flow, the devices operate in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if $\overline{CEAB}$ is low and CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB if $\overline{CEAB}$ is also low. $\overline{OEAB}$ is active low. When $\overline{OEAB}$ is low, the outputs are active. When $\overline{OEAB}$ is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that for A to B but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CEBA}$.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54GTL16612 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74GTL16612 is characterized for operation from −40°C to 85°C.

Widebus and UBT are trademarks of Texas Instruments Incorporated.

FUNCTION TABLE†

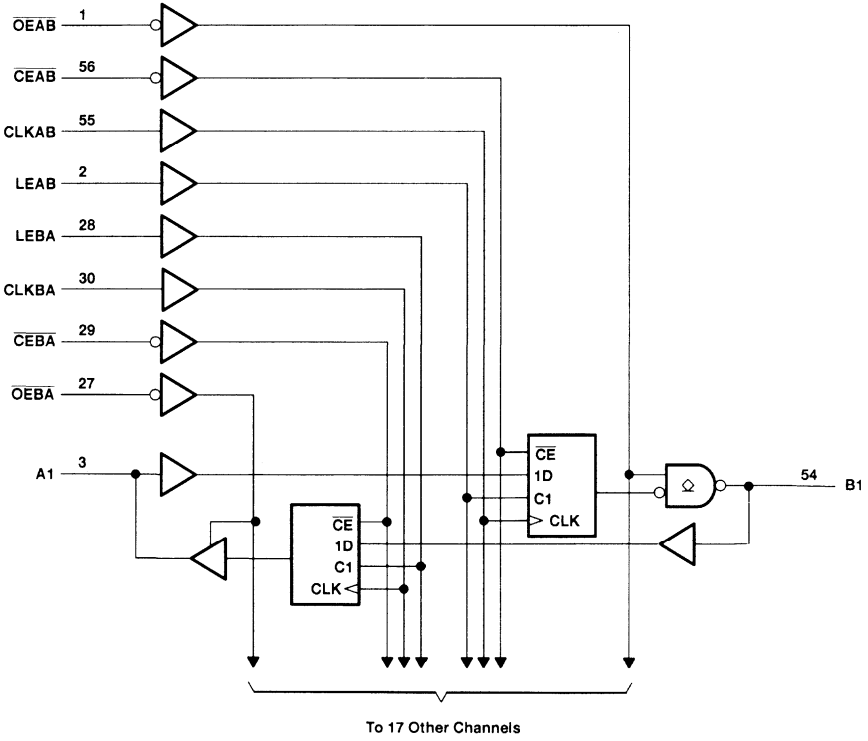
INPUTS					OUTPUT B	MODE
$\overline{CEAB}$	$\overline{OEAB}$	LEAB	CLKAB	A		
X	H	X	X	X	Z	Latched storage of A data
L	L	L	H	X	B_0‡	
L	L	L	L	X	B_0§	
X	L	H	X	L	L	Transparent
X	L	H	X	H	H	
L	L	L	↑	L	L	Clocked storage of A data
L	L	L	↑	H	H	
H	L	L	X	X	B_0§	Clock inhibit

† A-to-B data flow is shown: B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CEBA}$.

‡ Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low.

§ Output level before the indicated steady-state input conditions were established.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}: 3.3 V ..... −0.5 V to 4.6 V
5 V ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1): A port ..... −0.5 V to 7 V
B port ..... −0.5 V to 4.6 V
Voltage range applied to any output in the high or power-off state, V_O (see Note 1): A port ..... −0.5 V to 7 V
B port ..... −0.5 V to 4.6 V
Current into any A-port output in the low state, I_O ..... 128 mA
Current into any B-port output in the low state, I_O ..... 80 mA
Current into any A-port output in the high state, I_O (see Note 2) ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 1 W
DL package ..... 1.4 W
Operating free-air temperature range, T_A: SN54GTL16612 ..... −55°C to 125°C
SN74GTL16612 ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 4)

			SN54GTL16612			SN74GTL16612			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage, 3.3 V		3.15	3.3	3.45	3.15	3.3	3.45	V
	Supply voltage, 5 V		4.75	5	5.25	4.75	5	5.25	
V_{REF}	Supply voltage			0.8			0.8		V
V_I	Input voltage	B port			V_{CC} (3.3 V)			V_{CC} (3.3 V)	V
		Except B port			5.5			5.5	
V_{IH}	High-level input voltage	B port	V_{REF} + 50 mV			V_{REF} + 50 mV			V
		Except B port	2			2			
V_{IL}	Low-level input voltage	B port			V_{REF} − 50 mV			V_{REF} − 50 mV	V
		Except B port			0.8			0.8	
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	High-level output current	A port			−32			−32	mA
I_{OL}	Low-level output current	A port			64			64	mA
		B port			40			40	
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 4: Unused or floating control inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range, V_{REF} = 0.8 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54GTL16612			SN74GTL16612			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} (3.3 V) = 3.15 V, V_{CC} (5 V) = 4.75 V	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	A port	V_{CC} = MIN to MAX‡,	I_{OH} = −100 μA	V_{CC} − 0.2			V_{CC} − 0.2			V
		V_{CC} (3.3 V) = 3.15 V, V_{CC} (5 V) = 4.75 V	I_{OH} = −8 mA	2.4			2.4			
			I_{OH} = −32 mA	2			2			
V_{OL}	A port	V_{CC} (3.3 V) = 3.15 V, V_{CC} (5 V) = 4.75 V	I_{OL} = 100 μA			0.2			0.2	V
			I_{OL} = 16 mA			0.4			0.4	
			I_{OL} = 32 mA			0.5			0.5	
			I_{OL} = 64 mA			0.55			0.55	
	B port	V_{CC} (3.3 V) = 3.15 V, V_{CC} (5 V) = 4.75 V	I_{OL} = 40 mA			0.4			0.4	
I_I	Control inputs	V_{CC} = 0 or MAX‡,	V_I = 5.5 V			10			10	μA
	A port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V	V_I = 5.5 V			20			20	
			V_I = V_{CC}			1			1	
			V_I = 0			−30			−30	
	B port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V	V_I = V_{CC} (3.3 V)			5			5	
			V_I = 0			−5			−5	
I_{off}	A port	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V			100			100	μA
$I_{I(hold)}$	A port	V_{CC} (3.3 V) = 3.15 V, V_{CC} (5 V) = 4.75 V	V_I = 0.8 V	75			75			μA
			V_I = 2 V	−75			−75			
I_{OZH}	A port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V	V_O = 3 V			1			1	μA
	B port		V_O = 1.2 V			10			10	
I_{OZL}	A port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V	V_O = 0.5 V			−1			−1	μA
	B port		V_O = 0.4 V			−10			−10	
I_{CC} (3.3 V)	A or B port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V, I_O = 0, V_I = V_{CC} (3.3 V) or GND	Outputs high			1			1	mA
			Outputs low			5			5	
			Outputs disabled			1			1	
I_{CC} (5 V)	A or B port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V, I_O = 0, V_I = V_{CC} (5 V) or GND	Outputs high			120			120	mA
			Outputs low			120			120	
			Outputs disabled			120			120	
ΔI_{CC}§		V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V, A or control inputs at V_{CC} (3.3 V) or GND, One input at 2.7 V				1			1	mA
C_i	Control inputs	V_I = 3.15 V or 0			3.5			3.5		pF
C_{io}	A port	V_O = 3.15 V or 0			12			12		pF
	B port	Per IEEE Standard 1149.0-1991			5			5		

† All typical values are at V_{CC} (3.3 V) = 3.3 V, V_{CC} (5 V) = 5 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature, V_{REF} = 0.8 V (unless otherwise noted)

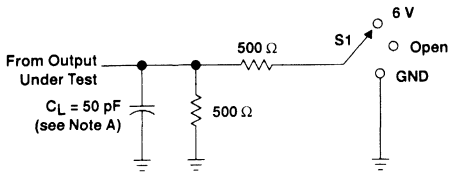
			SN54GTL16612		SN74GTL16612		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	95	0	95	MHz
t_w	Pulse duration	LEAB or LEBA high	3.3		3.3		ns
		CLKAB or CLKBA high or low	5.6		5.6		
t_{su}	Setup time	A before CLKAB↑	0.9		0		ns
		B before CLKBA↑	3.4		2.5		
		A before LEAB↓	1.2		0.4		
		B before LEBA↓	1		0.9		
		$\overline{CEAB}$ before CLKAB↑	2.1		1		
		$\overline{CEBA}$ before CLKBA↑	2.6		2.1		
t_h	Hold time	A after CLKAB↑	2.9		2.7		ns
		B after CLKBA↑	4.1		0.4		
		A after LEAB↓	4.5		3.4		
		B after LEBA↓	4.3		3.3		
		$\overline{CEAB}$ after CLKAB↑	2		1.5		
		$\overline{CEBA}$ after CLKBA↑	0.5		0.4		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{REF} = 0.8 V (see Figure 1)

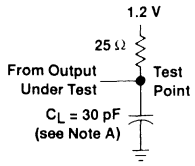
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54GTL16612			SN74GTL16612			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}			95			95			MHz
t_{PLH}	A	B	1	2.6	3.8	1	2.6	3.8	ns
t_{PHL}			1	2.2	4	1	2.2	4	
t_{PLH}	LEAB	B	1.8	3.6	5.4	1.8	3.6	5.4	ns
t_{PHL}			1.5	3.3	5.5	1.5	3.3	5.5	
t_{PLH}	CLKAB	B	1.8	3.7	5.3	1.8	3.7	5.3	ns
t_{PHL}			1.5	3.3	5.5	1.5	3.3	5.5	
t_{PLH}	$\overline{OEAB}$	B	1.6	3.3	4.7	1.6	3.3	4.7	ns
t_{PHL}			1.3	3.2	5.5	1.3	3.2	5.5	
t_r	Transition time, B outputs (0.5 V to 1 V)			1.3			1.3		ns
t_f	Transition time, B outputs (1 V to 0.5 V)			0.5			0.5		ns
t_{PLH}	B	A	2	4.8	6.9	2	4.8	6.9	ns
t_{PHL}			1.4	3.6	5.1	1.4	3.6	5.1	
t_{PLH}	LEBA	A	2.1	4.3	6.1	2.1	4.3	6.1	ns
t_{PHL}			1.9	3.6	5.1	1.9	3.6	5.1	
t_{PLH}	CLKBA	A	2.3	4.5	6.4	2.3	4.5	6.4	ns
t_{PHL}			2.2	4	5.6	2.2	4	5.6	
t_{en}	$\overline{OEBA}$	A	1.9	4.7	7.2	1.9	4.7	7.2	ns
t_{dis}			2.5	4.6	6.9	2.5	4.6	6.9	

† All typical values are at V_{CC} (3.3 V) = 3.3 V, V_{CC} (5 V) = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

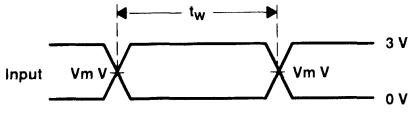


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

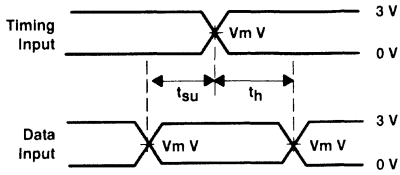


LOAD CIRCUIT FOR A OUTPUTS

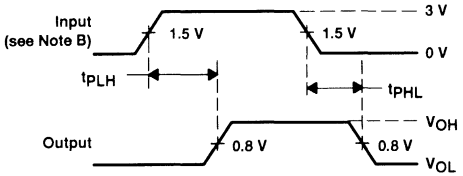
LOAD CIRCUIT FOR B OUTPUTS



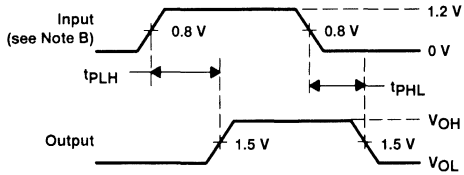
VOLTAGE WAVEFORMS
PULSE DURATION
(Vm = 1.5 V for A port and 0.8 V for B port)



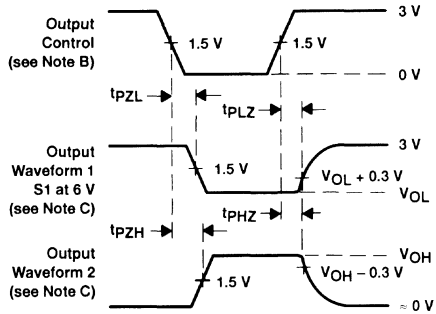
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
(Vm = 1.5 V for A port and 0.8 V for B port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(A port to B port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(B port to A port)



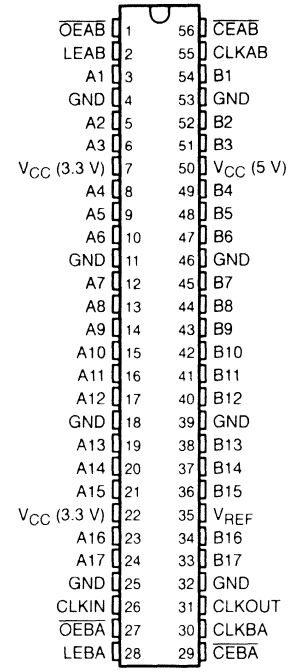
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(A port)

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

- **Translates Between GTL Signal Levels and LVTTL or 5-V TTL Signal Levels**
- **Members of the Texas Instruments *Widebus*™ Family**
- **Supports Mixed-Mode Signal Operation on A Port**
- **Universal Bus Transceiver (*UBT*™) Combines D-Type Latches and D-Type Flip-Flops With Qualified Storage Enable**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors on A Port**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Package Options Include Plastic Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Ceramic Flat (WD) Packages**

SN54GTL16616 . . . WD PACKAGE
SN74GTL16616 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

These 17-bit registered bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes. The 'GTL16616 provides for a copy of CLKAB at GTL logic levels (CLKOUT) and also provides a conversion of the GTL clock to a TTL environment (CLKIN).

The B port operates at GTL levels while the A port and control pins are compatible with LVCMOS, LVTTL, or 5-V TTL logic levels.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock or latch-enable can be controlled by the clock-enable ($\overline{CEAB}$ and $\overline{CEBA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if $\overline{CEAB}$ is low and CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB if $\overline{CEAB}$ is also low. $\overline{OEAB}$ is active low. When $\overline{OEAB}$ is low, the outputs are active. When $\overline{OEAB}$ is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that of A to B but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CEBA}$.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74GTL16616 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54GTL16616 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74GTL16616 is characterized for operation from −40°C to 85°C.

Widebus and UBT are trademarks of Texas Instruments Incorporated.

TEXAS INSTRUMENTS

FUNCTION TABLE†

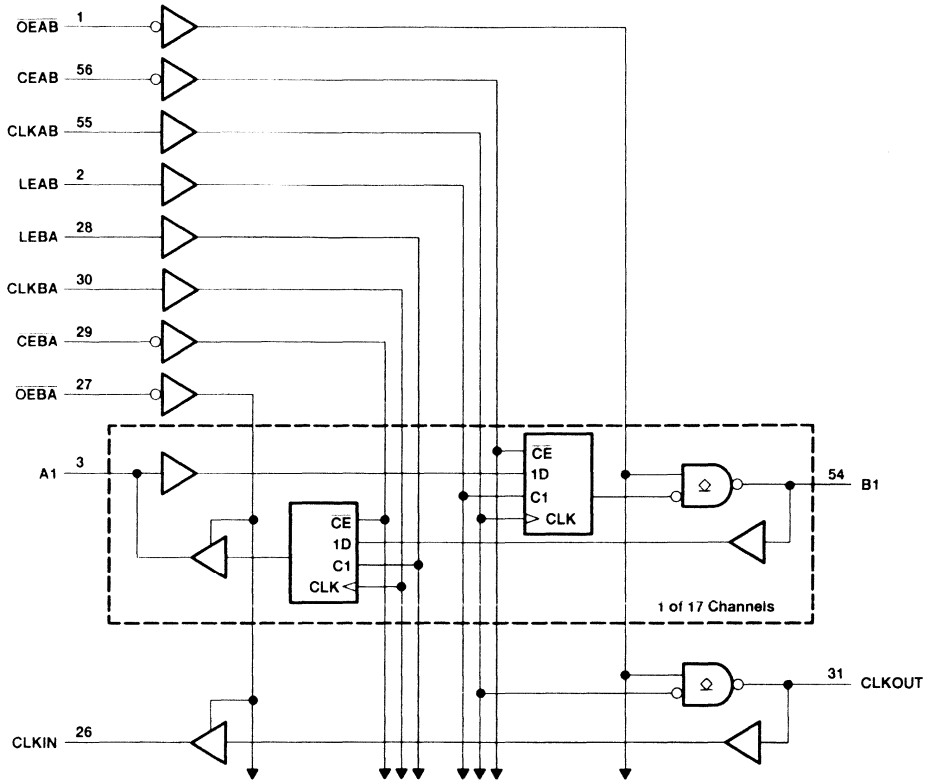
INPUTS					OUTPUT B	MODE
$\overline{CEAB}$	OEAB	LEAB	CLKAB	A		
X	H	X	X	X	Z	Latched storage of A data
L	L	L	H or L	X	B_0‡	
L	L	L	H or L	X	B_0§	
X	L	H	X	L	L	Transparent
X	L	H	X	H	H	
L	L	L	↑	L	L	Clocked storage of A data
L	L	L	↑	H	H	
H	L	L	X	X	B_0§	Clock inhibit

† A-to-B data flow is shown: B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, $\overline{CLKBA}$, and $\overline{CEBA}$.

‡ Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low.

§ Output level before the indicated steady-state input conditions were established.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}: 3.3 V ..... –0.5 V to 4.6 V
5 V ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1): A port ..... –0.5 V to 7 V
B port ..... –0.5 V to 4.6 V
Voltage range applied to any output in the high or power-off state, V_O (see Note 1): A port ..... –0.5 V to 7 V
B port ..... –0.5 V to 4.6 V
Current into any A-port output in the low state, I_O ..... 128 mA
Current into any B-port output in the low state, I_O ..... 80 mA
Current into any A-port output in the high state, I_O (see Note 2) ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... –50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... –50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will flow only when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 4)

			SN54GTL16616			SN74GTL16616			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage, 3.3 V		3.15	3.3	3.45	3.15	3.3	3.45	V
	Supply voltage, 5 V		4.75	5	5.25	4.75	5	5.25	
V_{REF}	Supply voltage			0.8			0.8		V
V_I	Input voltage	B port			V_{CC} (3.3 V)			V_{CC} (3.3 V)	V
		Except B port			5.5			5.5	
V_{IH}	High-level input voltage	B port	V_{REF} +50 mV			V_{REF} +50 mV			V
		Except B port	2			2			
V_{IL}	Low-level input voltage	B port			V_{REF} –50 mV			V_{REF} –50 mV	V
		Except B port			0.8			0.8	
I_{IK}	Input clamp current				–18			–18	mA
I_{OH}	High-level output current	A port			–32			–32	mA
I_{OL}	Low-level output current	A port			64			64	mA
		B port			40			40	
T_A	Operating free-air temperature		–55		125	–40		85	°C

NOTE 4: Unused or floating control inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range, V_{REF} = 0.8 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54GTL16616			SN74GTL16616			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} (3.3 V) = 3.15 V, V_{CC} (5 V) = 4.75 V	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	A port	V_{CC} = MIN to MAX‡,	I_{OH} = −100 μA	V_{CC} − 0.2			V_{CC} − 0.2			V
		V_{CC} (3.3 V) = 3.15 V, V_{CC} (5 V) = 4.75 V	I_{OH} = −8 mA	2.4			2.4			
			I_{OH} = −32 mA	2			2			
V_{OL}	A port	V_{CC} (3.3 V) = 3.15 V, V_{CC} (5 V) = 4.75 V	I_{OL} = 100 μA			0.2			0.2	V
			I_{OL} = 16 mA			0.4			0.4	
			I_{OL} = 32 mA			0.5			0.5	
			I_{OL} = 64 mA			0.55			0.55	
	B port	V_{CC} (3.3 V) = 3.15 V, V_{CC} (5 V) = 4.75 V	I_{OL} = 40 mA			0.4			0.4	
I_I	Control inputs	V_{CC} = 0 or MAX‡,	V_I = 5.5 V			10			10	μA
	A port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V	V_I = 5.5 V			20			20	
			V_I = V_{CC}			1			1	
			V_I = 0			−30			−30	
	B port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V	V_I = V_{CC} (3.3 V)			5			5	
			V_I = 0			−5			−5	
I_{off}	A port	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V			100			100	μA
$I_{I(hold)}$	A port	V_{CC} (3.3 V) = 3.15 V, V_{CC} (5 V) = 4.75 V	V_I = 0.8 V	75			75			μA
			V_I = 2 V	−75			−75			
I_{OZH}	A port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V	V_O = 3 V			1			1	μA
	B port		V_O = 1.2 V			10			10	
I_{OZL}	A port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V	V_O = 0.5 V			−1			−1	μA
	B port		V_O = 0.4 V			−10			−10	
I_{CC} (3.3 V)	A or B port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V, I_O = 0, V_I = V_{CC} (3.3 V) or GND	Outputs high			1			1	mA
			Outputs low			5			5	
			Outputs disabled			1			1	
I_{CC} (5 V)	A or B port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V, I_O = 0, V_I = V_{CC} (5 V) or GND	Outputs high			120			120	mA
			Outputs low			120			120	
			Outputs disabled			120			120	
ΔI_{CC}§		V_{CC} (3.3 V) = 3.45 V, A or control inputs at V_{CC} (3.3 V) or GND, One input at 2.7 V	V_{CC} (5 V) = 5.25 V,			1			1	mA
C_i	Control inputs	V_I = 3.15 V or 0			3.5			3.5		pF
C_{io}	A port	V_O = 3.15 V or 0			12			12		pF
	B port	Per IEEE 1194.0-1991				5			5	

† All typical values are at V_{CC} (3.3 V) = 3.3 V, V_{CC} (5 V) = 5 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature, V_{REF} = 0.8 V (unless otherwise noted)

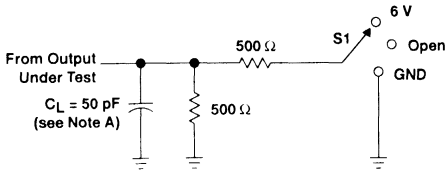
			SN54GTL16616		SN74GTL16616		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	95	0	95	MHz
t_w	Pulse duration	LEAB or LEBA high	3.3		3.3		ns
		CLKAB or CLKBA high or low	5.5		5.5		
t_{su}	Setup time	A before CLKAB↑	1.1		1.1		ns
		B before CLKBA↑	2.6		2.6		
		A before LEAB↓	0		0		
		B before LEBA↓	1		1		
		$\overline{CEAB}$ before CLKAB↑	1.8		1.8		
		$\overline{CEBA}$ before CLKBA↑	2.1		2.1		
t_h	Hold time	A after CLKAB↑	1.6		1.6		ns
		B after CLKBA↑	0.2		0.2		
		A after LEAB↓	4.3		4.3		
		B after LEBA↓	2.8		2.8		
		$\overline{CEAB}$ after CLKAB↑	0.8		0.8		
		$\overline{CEBA}$ after CLKBA↑	0.7		0.7		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{REF} = 0.8 V (see Figure 1)

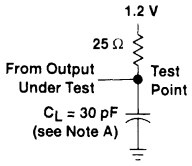
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54GTL16616			SN74GTL16616			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}			95			95			MHz
t_{PLH}	A	B	1	2.5	3.8	1	2.5	3.8	ns
t_{PHL}			1	2	3.8	1	2	3.8	
t_{PLH}	LEAB	B	1.5	3.4	5.1	1.5	3.4	5.1	ns
t_{PHL}			1.4	3.2	5.1	1.4	3.2	5.1	
t_{PLH}	CLKAB	B	1.5	3.6	5	1.5	3.6	5	ns
t_{PHL}			1.4	4.1	5	1.4	4.1	5	
t_{PLH}	CLKAB	CLKOUT	3.4	6	7.7	3.4	6	7.7	ns
t_{PHL}			4.3	7.4	10.4	4.3	7.4	10.4	
t_{PLH}	$\overline{OEAB}$	B	1.3	3.2	5	1.3	3.2	5	ns
t_{PHL}			1.1	3.1	5	1.1	3.1	5	
t_r	Transition time, B outputs (0.5 V to 1 V)			1.2			1.2		ns
t_f	Transition time, B outputs (1 V to 0.5 V)			0.7			0.7		ns
t_{PLH}	B	A	2.1	4.4	6.5	2.1	4.4	6.5	ns
t_{PHL}			1.3	3.3	4.8	1.3	3.3	4.8	
t_{PLH}	LEBA	A	1.7	3.9	6	1.7	3.9	6	ns
t_{PHL}			1.3	3.3	4.6	1.3	3.3	4.6	
t_{PLH}	CLKBA	A	1.7	4.1	6.3	1.7	4.1	6.3	ns
t_{PHL}			1.4	3.6	5.3	1.4	3.6	5.3	
t_{PLH}	CLKOUT	CLKIN	6.5	10.5	14.3	6.5	10.5	14.3	ns
t_{PHL}			5.1	8.8	11.8	5.1	8.8	11.8	
t_{en}	$\overline{OEBA}$	A	1.8	4.7	6.9	1.8	4.7	6.9	ns
t_{dis}			2	4.7	6.7	2	4.7	6.7	

† All typical values are at V_{CC} (3.3 V) = 3.3 V, V_{CC} (5 V) = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

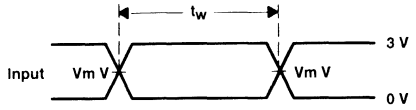


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

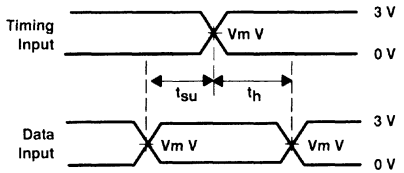


LOAD CIRCUIT FOR A OUTPUTS

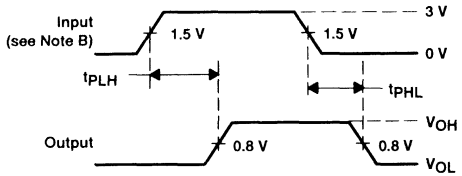
LOAD CIRCUIT FOR B OUTPUTS



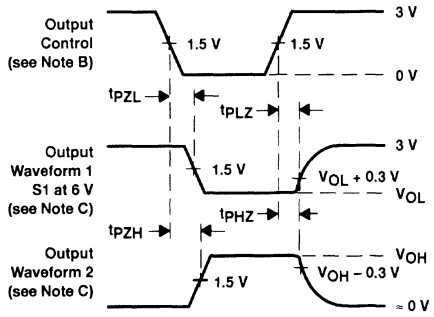
VOLTAGE WAVEFORMS
PULSE DURATION
(Vm = 1.5 V for A port and 0.8 V for B port)



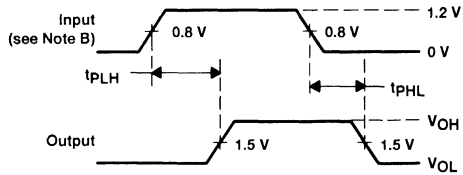
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
(Vm = 1.5 V for A port and 0.8 V for B port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(A port to B port)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(A port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(B port to A port)

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

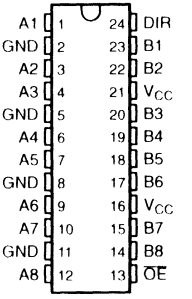
Today designers are often faced with the problem of bus interface circuits having insufficient drive capability when driving low-impedance bus lines. Transmission lines with a characteristic impedance of less than 30 ohms are no longer a rarity (mainframe computers; switching systems; industrial control systems). If the necessary output current cannot be provided the result will generally be a reduction in system speed.

As the line impedance can hardly by influenced, the driver needs to provide sufficient drive capability. In other words, the driver output needs to provide a sufficiently high amount of current to switch the bus or the line directly from one logic state to the other (incident wave switching, IWS). Otherwise, it takes several wave reflections until the line signal level reaches the desired logic level.

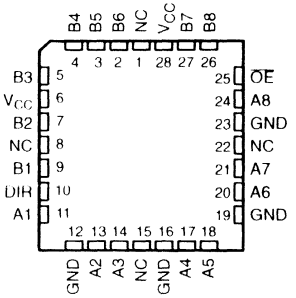
To support IWS on highly-loaded lines, TI has developed several BiCMOS functions, designated SN74BCT25xxx, which offer an extended output drive of $I_{o}l$ – 188 mA and $I_{o}h$ = 80 mA, which is sufficient for reliable operation of lines with impedances down to 25 ohms.

- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **Designed to Facilitate Incident-Wave Switching for Line Impedances of 25 Ω or Greater**
- **Distributed V_{CC} and GND Pins Minimize Noise Generated by the Simultaneous Switching of Outputs**
- **Bus-Hold Inputs Eliminate the Need for External Pullup Resistors**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

SN54ABT25245 . . . JT PACKAGE
SN74ABT25245 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54ABT25245 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'ABT25245 is a 25-Ω octal bus transceiver designed for asynchronous communication between data buses. It improves both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented transceivers.

The device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can disable the device so that both buses are effectively isolated.

This transceiver is capable of sinking 188 mA of I_{OL} current, which facilitates switching 25-Ω transmission lines on the incident wave. The distributed V_{CC} and GND pins minimize switching noise for more reliable system operation.

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT25245 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ABT25245 is characterized for operation from −40°C to 85°C.

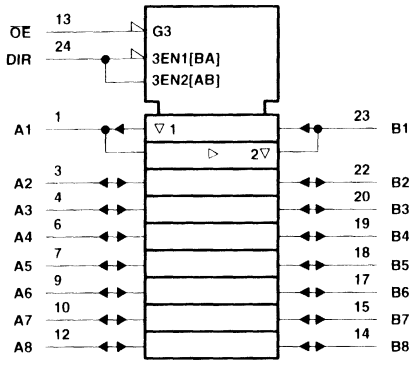
EPIC-IIB is a trademark of Texas Instruments Incorporated.

TEXAS INSTRUMENTS

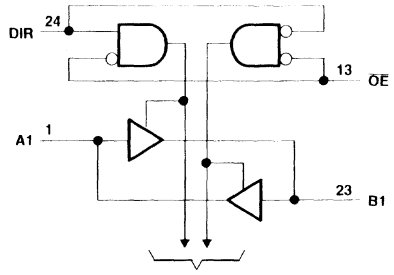
FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, V_O ..... −0.5 V to 5.5 V
Voltage range applied to any output in the high state, V_O ..... −0.5 V to V_{CC}
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Current into any output in the low state, I_O: SN54ABT25245 (A port) ..... 250 mA
SN54ABT25245 (B port) ..... 96 mA
SN74ABT25245 (A port) ..... 376 mA
SN74ABT25245 (B port) ..... 128 mA
Operating free-air temperature range: SN54ABT25245 ..... −55°C to 125°C
SN74ABT25245 ..... −40°C to 85°C
Maximum power dissipation at T_A = 55°C (in still air): DW package ..... 1 W
NT package ..... 1.3 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

				SN54ABT25245		SN74ABT25245		UNIT
				MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage			4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage			2		2		V
V_{IL}	Low-level input voltage				0.8		0.8	V
V_I	Input voltage			0	V_{CC}	0	V_{CC}	V
I_{IK}	Input clamp current				−18		−18	mA
I_{OH}	High-level output current		A ports		−53		−80	mA
			B ports		−24		−32	
I_{OL}	Low-level output current		A ports		125		188	mA
			B ports		48		64	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled	Control inputs		4		4	ns/V
			A or B ports		10		10	
T_A	Operating free-air temperature			−55	125	−40	85	C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

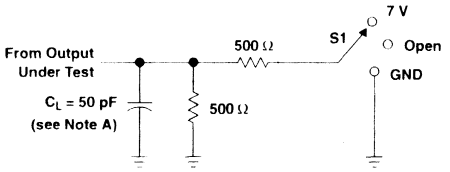
PARAMETER		TEST CONDITIONS		SN54ABT25245			SN74ABT25245			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V, I_I = −18 mA				−1.2			−1.2	V
V_{OH}	A ports	V_{CC} = 4.75 V, I_{OH} = −3 mA					2.7			V
		V_{CC} = 4.5 V, I_{OH} = −53 mA		2						
		V_{CC} = 4.5 V, I_{OH} = −80 mA					2.4			
	B ports	V_{CC} = 4.5 V, I_{OH} = −3 mA		2.5			2.5			
		V_{CC} = 5 V, I_{OH} = −3 mA		3			3			
		V_{CC} = 4.5 V, I_{OH} = −32 mA					2			
V_{OL}	A ports	V_{CC} = 4.5 V, I_{OL} = 94 mA				0.55			0.55	V
		V_{CC} = 4.5 V, I_{OL} = 125 mA				0.8				
		V_{CC} = 4.5 V, I_{OL} = 188 mA							0.7	
	B ports	V_{CC} = 4.5 V, I_{OL} = 55 mA				0.55				
		V_{CC} = 4.5 V, I_{OL} = 64 mA							0.55	
I_I	Control inputs	V_{CC} = 5.5 V, V_I = V_{CC} or GND				±1			±1	µA
	A or B ports					±100			±100	
I_{hold}	A or B ports	V_{CC} = 4.5 V, V_I = 0.8 V		100			100			µA
		V_{CC} = 4.5 V, V_I = 2 V		−100			−100			
I_{OZH}‡		V_{CC} = 5.5 V, V_O = 2.7 V				50			50	µA
I_{OZL}‡		V_{CC} = 5.5 V, V_O = 0.5 V				−50			−50	µA
I_{OFF}		V_{CC} = 0, V_I or V_O ≤ 4.5 V				±500			±100	µA
I_{CEX}		V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50			50	µA
I_O§	B ports	V_{CC} = 5.5 V, V_O = 2.5 V		−50		−210	−50		−210	mA
I_{CC}		V_{CC} = 5.5 V, Outputs open, V_I = V_{CC} or GND	Outputs high			500			500	µA
			Outputs low			20			20	mA
			Outputs disabled			500			500	µA
ΔI_{CC}¶		V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				1			1	mA
C_i	Control inputs	V_{CC} = 5 V, V_I = V_{CC} or GND			4			4		pF
C_{io}	A or B ports	V_{CC} = 5 V, V_O = V_{CC} or GND			11.5			11.5		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

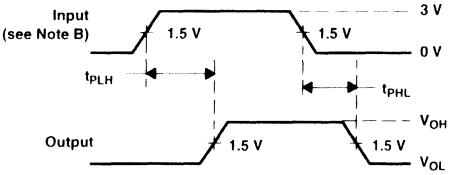
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT25245		SN74ABT25245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1	2.3	3.5	1	4	1	3.9	ns
t_{PHL}			1	2.4	3.5	1	4.5	1	4.3	
t_{PZH}	$\overline{OE}$	A or B	1.5	3.7	5.4	1.5	6.8	1.5	6.5	ns
t_{PZL}			1.4	4	5.8	1.4	7.1	1.4	6.8	
t_{PHZ}	$\overline{OE}$	A or B	2	4.3	6.1	2	7.4	2	7.2	ns
t_{PLZ}			2	3.9	5.8	2	7.3	2	6.4	

PARAMETER MEASUREMENT INFORMATION

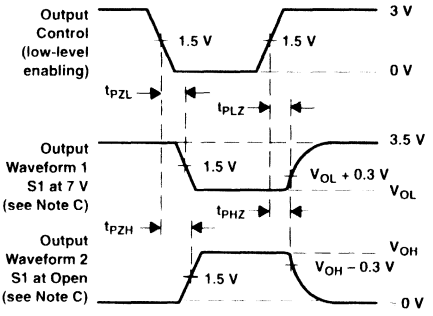


LOAD CIRCUIT FOR OUTPUTS

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



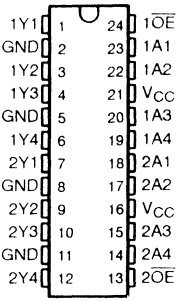
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

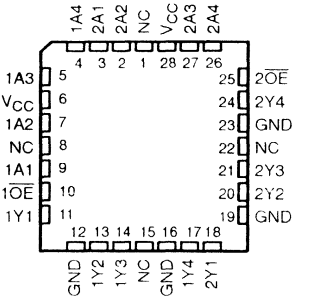
Figure 1. Load Circuit and Voltage Waveforms

- State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Designed to Facilitate Incident-Wave Switching for Line Impedances of 25 Ω or Greater
- Distributed V_{CC} and GND Pins Minimize Noise Generated by the Simultaneous Switching of Outputs
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

SN54BCT25244 . . . JT PACKAGE
SN74BCT25244 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54BCT25244 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These 25-Ω octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

These buffers are capable of sinking a 188-mA I_{OL}, which facilitates switching 25-Ω transmission lines on the incident wave. The distributed V_{CC} and GND pins minimize switching noise for more reliable system operation.

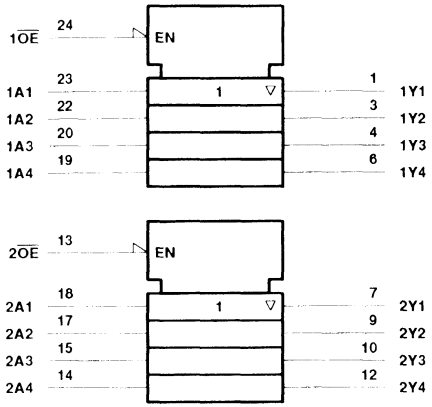
When the output-enable ($1\overline{OE}$ and $2\overline{OE}$) inputs are low, the device transmits data from the A inputs to the Y outputs. When $1\overline{OE}$ and $2\overline{OE}$ are high, the outputs are in the high-impedance state.

The SN54BCT25244 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74BCT25244 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(EACH BUFFER/DRIVER)

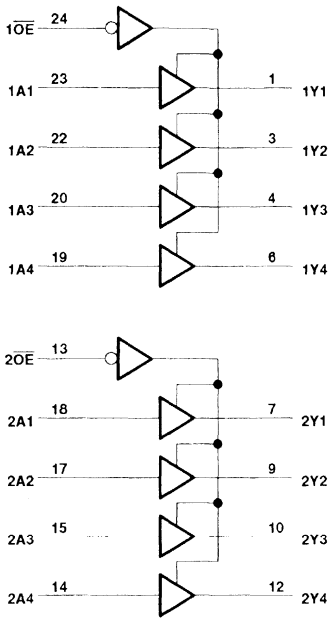
INPUTS		OUTPUT
$\overline{OE}$	A	Y
H	X	Z
L	L	L
L	H	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state, V_O . . . . . –0.5 V to 5.5 V
Voltage applied to any output in the high state, V_O . . . . . –0.5 V to V_{CC}
Input clamp current, I_{IK} ($V_I < 0$) . . . . . –30 mA
Current into any output in the low state, I_O: SN54BCT25244 . . . . . 250 mA
SN74BCT25244 . . . . . 376 mA
Operating free-air temperature range: SN54BCT25244 . . . . . –55°C to 125°C
SN74BCT25244 . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

Pin numbers shown are for DW, JT, and NT packages.

recommended operating conditions (see Note 2)

		SN54BCT25244			SN74BCT25244			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			–18			–18	mA
I_{OH}	High-level output current			–53			–80	mA
I_{OL}	Low-level output current			125			188	mA
T_A	Operating free-air temperature	–55		125	0		70	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

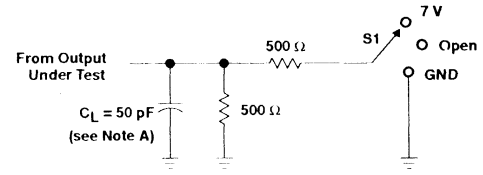
PARAMETER	TEST CONDITIONS		SN54BCT25244			SN74BCT25244			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA			–1.2			–1.2	V
V_{OH}	V_{CC} = 4.75 V,	I_{OH} = –3 mA				2.7			V
	V_{CC} = 4.5 V,	I_{OH} = –53 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = –80 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 94 mA		0.38	0.55		0.42	0.55	V
	V_{CC} = 4.5 V,	I_{OL} = 125 mA			0.8				
	V_{CC} = 4.5 V,	I_{OL} = 188 mA						0.7	
I_I	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			–0.6			–0.6	mA
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	µA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V			–50			–50	µA
I_{CCL}	V_{CC} = 5.5 V,	Outputs open		90	119		90	119	mA
I_{CCH}	V_{CC} = 5.5 V,	Outputs open		59	78		59	78	mA
I_{CCZ}	V_{CC} = 5.5 V,	Outputs open		7	11		7	11	mA
C_i	V_{CC} = 5 V,	V_I = V_{CC} or GND		5.5			5.5		pF
C_o	V_{CC} = 5 V,	V_O = V_{CC} or GND		17			17		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

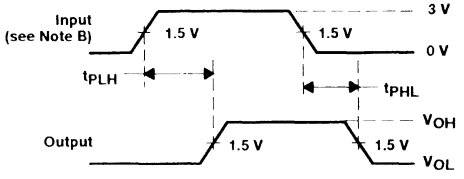
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54BCT25244		SN74BCT25244		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1	3.2	4.9	1	5.8	1	5.5	ns
t_{PHL}			2	4	5.6	2	6.3	2	6	
t_{PZH}	$\overline{OE}$	Y	3.2	5.6	8.5	3.2	9.7	3.2	9.3	ns
t_{PZL}			3.7	6.3	9.2	3.7	10.4	3.7	10.2	
t_{PHZ}	$\overline{OE}$	Y	1.6	3.6	5.5	1.6	6.5	1.6	6.3	ns
t_{PLZ}			3.1	5.3	7.8	3.1	9.5	3.1	8.4	

PARAMETER MEASUREMENT INFORMATION

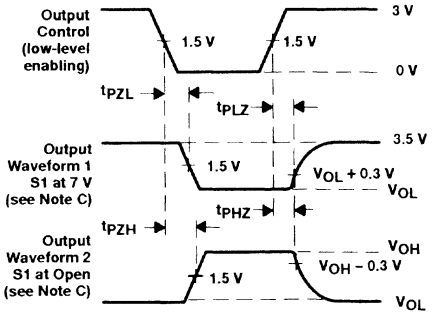


LOAD CIRCUIT FOR OUTPUTS

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



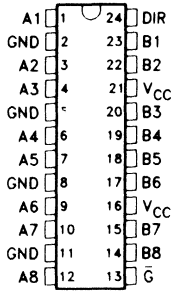
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

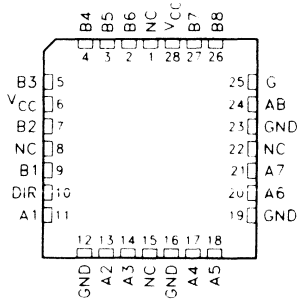
Figure 1. Load Circuit and Voltage Waveforms

- **State-of-the-Art BICMOS Design Significantly Reduces I_{CCZ}**
- **Designed to Facilitate Incident Wave Switching for Line Impedances of 25-Ohm or Greater**
- **Distributed V_{CC} and GND Pins Minimize Noise Generated by the Simultaneous Switching of Outputs**
- **Data Flow-Through Pinout (All Inputs on Opposite Side from Outputs)**
- **ESD Protection Exceeds 2000 V per Mil-Std-883C Method 3015**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

SN54BCT25245 . . . JT PACKAGE
SN74BCT25245 . . . DW or NT PACKAGE
(TOP VIEW)



SN54BCT25245 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

These 25-ohm octal bus transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input $\overline{G}$ can be used to disable the device so that the buses are effectively isolated.

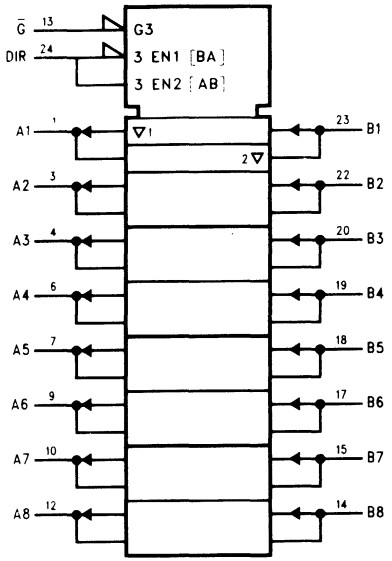
These transceivers are capable of sinking 188 mA of I_{OL} current (A port), which facilitates switching 25-ohm transmission lines on the incident wave. They are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented transceivers. The distributed V_{CC} and GND pins minimize the noise generated by the simultaneous switching of the outputs.

The SN54BCT25245 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74BCT25245 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

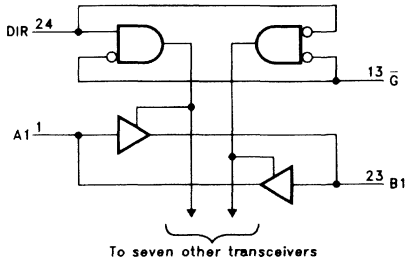
ENABLE INPUTS		OPERATION
$\overline{G}$	DIR	'BCT25245
L	L	B Data to A Bus
L	H	A Data to B Bus
H	X	Isolation

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range (see Note 1): Control Inputs ..... −0.5 V to 7 V
I/O ports ..... −0.5 V to 5.5 V
Voltage applied to any output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage applied to any output in the high state (B port) ..... −0.5 V to V_{CC}
Input clamp current ..... −30 mA
Current into any output in the low state: SN54BCT25245 (A port) ..... 250 mA
(B port) ..... 40 mA
SN74BCT25245 (A port) ..... 376 mA
(B port) ..... 48 mA
Operating free-air temperature range: SN54BCT25245 ..... −55°C to 125°C
SN74BCT25245 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			'54BCT25245			'74BCT25245			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	High-level output current	A1-A8			−53			−80	mA
		B1-B8			−3			−3	
I_{OL}	Low-level output current	A1-A8			125			188	mA
		B1-B8			20			24	
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'54BCT25245			'74BCT25245			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V, I_I = −18 mA			−1.2			−1.2	V
V_{OH}	Any A	V_{CC} = 4.5 V, I_{OH} = −53 mA	2						V
		V_{CC} = 4.5 V, I_{OH} = −80 mA				2			
		V_{CC} = 4.75 V, I_{OH} = −3 mA				2.7			
	Any B	V_{CC} = 4.5 V, I_{OH} = −3 mA	2.4	3.3		2.4	3.3		
V_{OL}	Any A	V_{CC} = 4.5 V, I_{OL} = 94 mA		0.38	0.55		0.42	0.55	V
		V_{CC} = 4.5 V, I_{OL} = 125 mA			0.8				
		V_{CC} = 4.5 V, I_{OL} = 188 mA						0.7	
	Any B	V_{CC} = 4.5 V, I_{OL} = 20 mA		0.3	0.5				
		V_{CC} = 4.5 V, I_{OL} = 24 mA					0.35	0.5	
I_I	A and B	V_{CC} = 5.5 V, V_I = 5.5 V			0.25			0.25	mA
	DIR and $\overline{G}$	V_{CC} = 5.5 V, V_I = 5.5 V			0.1			0.1	
I_{IH}‡	A and B	V_{CC} = 5.5 V, V_I = 2.7 V			70			70	μA
	DIR and $\overline{G}$	V_{CC} = 5.5 V, V_I = 2.7 V			20			20	
I_{IL}‡	A and B	V_{CC} = 5.5 V, V_I = 0.5 V			−0.6			−0.6	mA
	DIR and $\overline{G}$	V_{CC} = 5.5 V, V_I = 0.5 V			−0.6			−0.6	
I_{OS}§	B port only¶	V_{CC} = 5.5 V, V_O = 0	−60		−150	−60		−150	mA
I_{CCH}	A to B	V_{CC} = 5.5 V		36	46		36	46	mA
	B to A			63	77		63	77	
I_{CCL}	A to B	V_{CC} = 5.5 V		48	60		48	60	mA
	B to A			95	115		95	115	
I_{CCZ}		V_{CC} = 5.5 V		12	16		12	16	mA
C_{in}	$\overline{G}$ and DIR	V_{CC} = 5.5 V, V_I = 2.5 V or 0.5 V		8			8		pF
C_{io}	A port	V_{CC} = 5.5 V, V_I = 2.5 V or 0.5 V		18			18		pF
	B port			8			8		

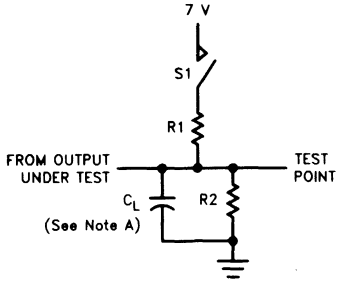
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
¶ Testing for this parameter on the A port is not recommended.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			'BCT25245			'54BCT25245		'74BCT25245		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1.2	3.3	5.1	1.2	5.8	1.2	5.7	ns
t_{PHL}			1.9	4.3	6.7	1.9	7.6	1.9	7.2	
t_{PLH}	B	A	1.2	3.3	4.8	1.2	5.7	1.2	5.5	ns
t_{PHL}			2.1	4	5.6	2.1	6.4	2.1	6.2	
t_{PZH}	$\overline{G}$	A	3.7	6.3	8.4	3.7	10.1	3.7	9.6	ns
t_{PZL}			4.5	7.4	9.2	4.5	11.1	4.5	10.3	
t_{PHZ}	$\overline{G}$	A	1.8	3.7	5.5	1.8	6.4	1.8	6.2	ns
t_{PLZ}			3.3	5.1	7.2	3.3	9.6	3.3	8.3	
t_{PZH}	$\overline{G}$	B	3.4	5.7	7.9	3.4	9.2	3.4	8.9	ns
t_{PZL}			4.3	6.6	8.7	4.3	10.1	4.3	9.7	
t_{PHZ}	$\overline{G}$	B	2.7	4.5	6.3	2.7	7.2	2.7	6.9	ns
t_{PLZ}			1.7	4.5	6.8	1.7	8.3	1.7	7.5	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

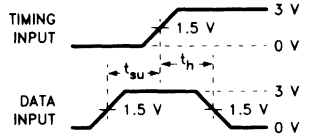
PARAMETER MEASUREMENT INFORMATION



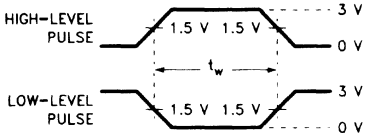
LOAD CIRCUIT FOR
3-STATE OUTPUTS

SWITCH POSITION TABLE

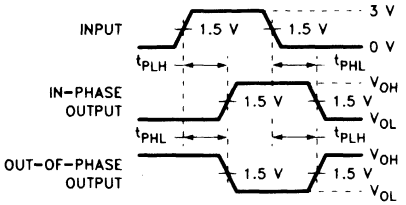
TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



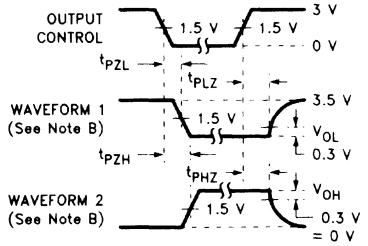
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



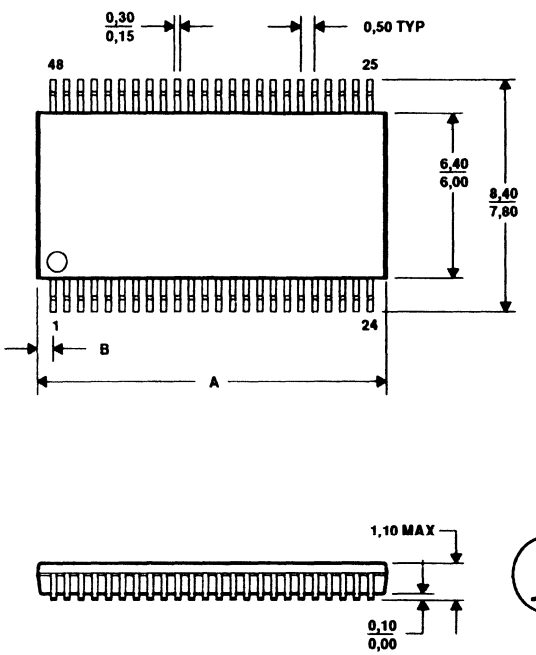
VOLTAGE WAVEFORMS
ENABLE AND DISABLED TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

DGG/R-PDSO-G**

300-MIL THIN SHRINK SMALL-OUTLINE PACKAGE



DIM \ PINS**	48	56
A MAX	12,80	14,30
A MIN	12,40	13,90
B MAX	0,65	0,40

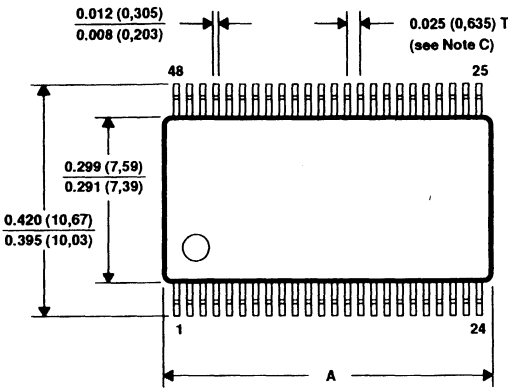
4040078/A–07/93

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions include mold flash or protrusion.

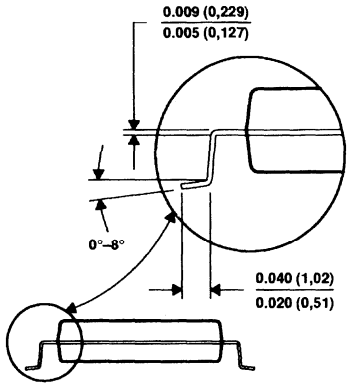
DL/R-PDSO-G**

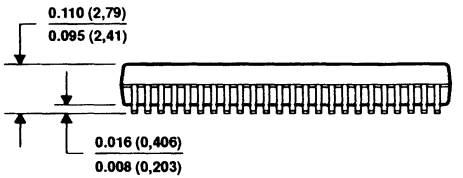
PLASTIC SHRINK SMALL-OUTLINE PACKAGE

48-PIN SHOWN



DIM \ PINS**	28	48	56
A MAX	0.380 (9,65)	0.630 (16,00)	0.730 (18,54)
A MIN	0.370 (9,40)	0.620 (15,75)	0.720 (18,29)



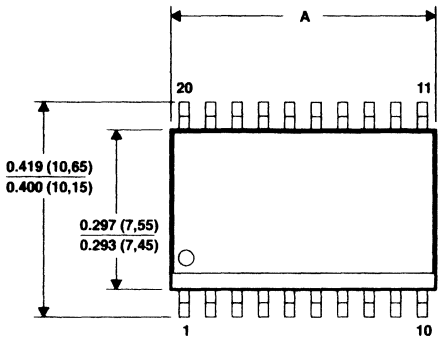


4040048/A–07/93

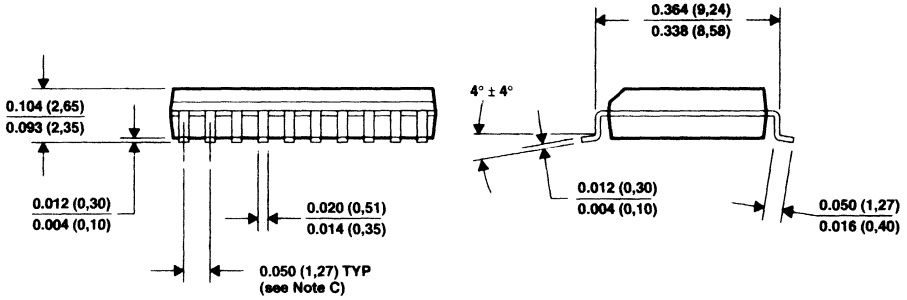
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Leads are within 0.0035 (0,089) radius of true postion at maximum material condition.
D. Body dimensions do not include mold flash , protrusion or gate burr.
E. Mold flash or protrusion or gate burr shall not exceed 0.015 (0,381).
F. Lead tips coplanar within 0.004 (0,102).
G. Lead length measured from lead top to point 0.010 (0,254) above seating plane.

DW/R-PDSO-G**
20-PIN SHOWN

PLASTIC WIDE-BODY SMALL-OUTLINE PACKAGE



DIM \ PINS**	16	20	24	28
A MIN	0.400 (10,16)	0.500 (12,70)	0.602 (15,29)	0.696 (17,68)
A MAX	0.408 (10,36)	0.508 (12,90)	0.610 (15,49)	0.704 (17,88)

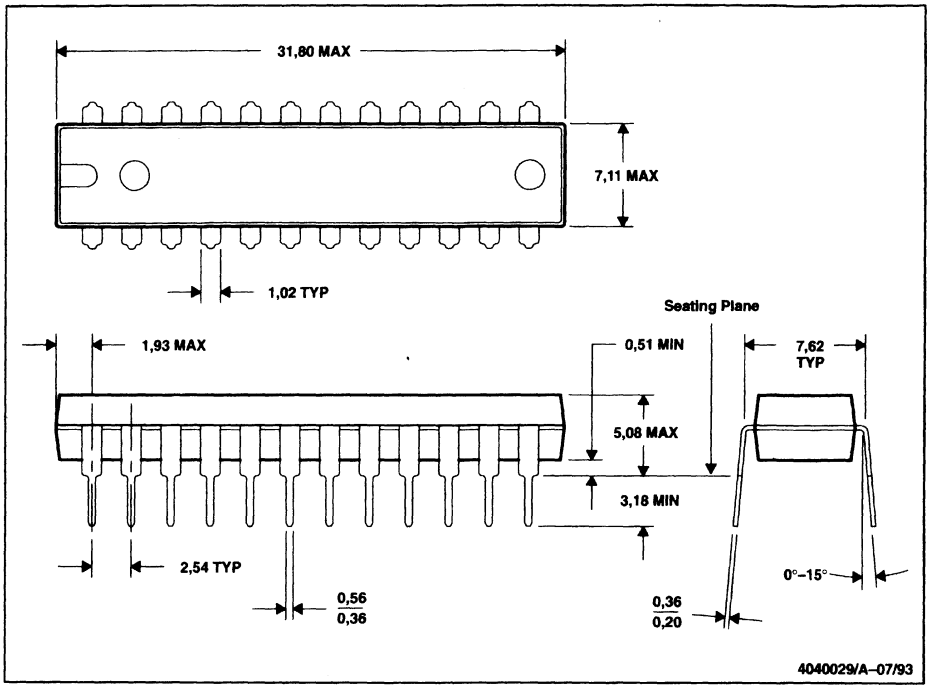


4040000/A–07/93

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Leads are within 0.10 (0,25) radius of true postion at maximum material condition.
D. Body dimensions do not include mold flash or protrusion.
E. Mold flash or protrusion shall not exceed 0.006 (0,15).
F. Lead tips coplanar within ±0.004 (±0,10) exclusive of solder.

MECHANICAL DATA

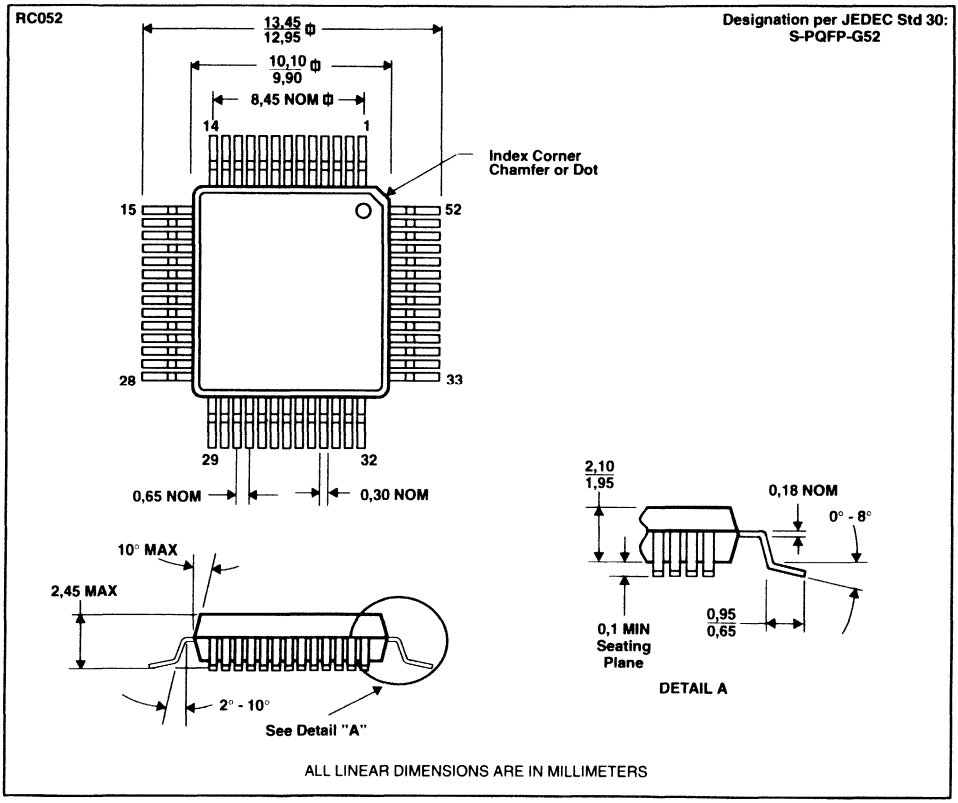
NT/R-PDIP-T24 **PLASTIC DUAL-IN-LINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Drawing source: SCJ Package handbook, 1990

RC052
plastic quad flatpack

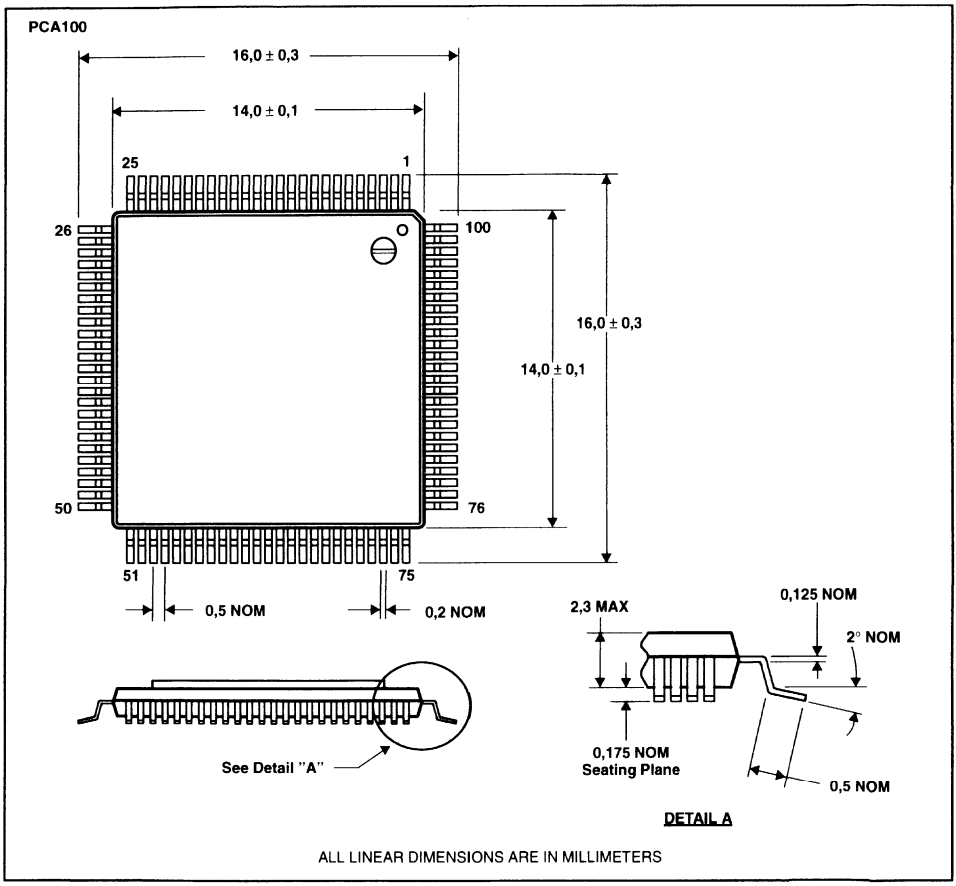
This plastic package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound withstands soldering temperatures with no deformation, and circuit performance characteristics remain stable when the devices are operated in high-humidity conditions. The package is intended for surface mounting and leads are spaced on 0,65 mm centers with an 0,80-mm foot length. Leads require no additional cleaning or processing when used in soldered assembly.



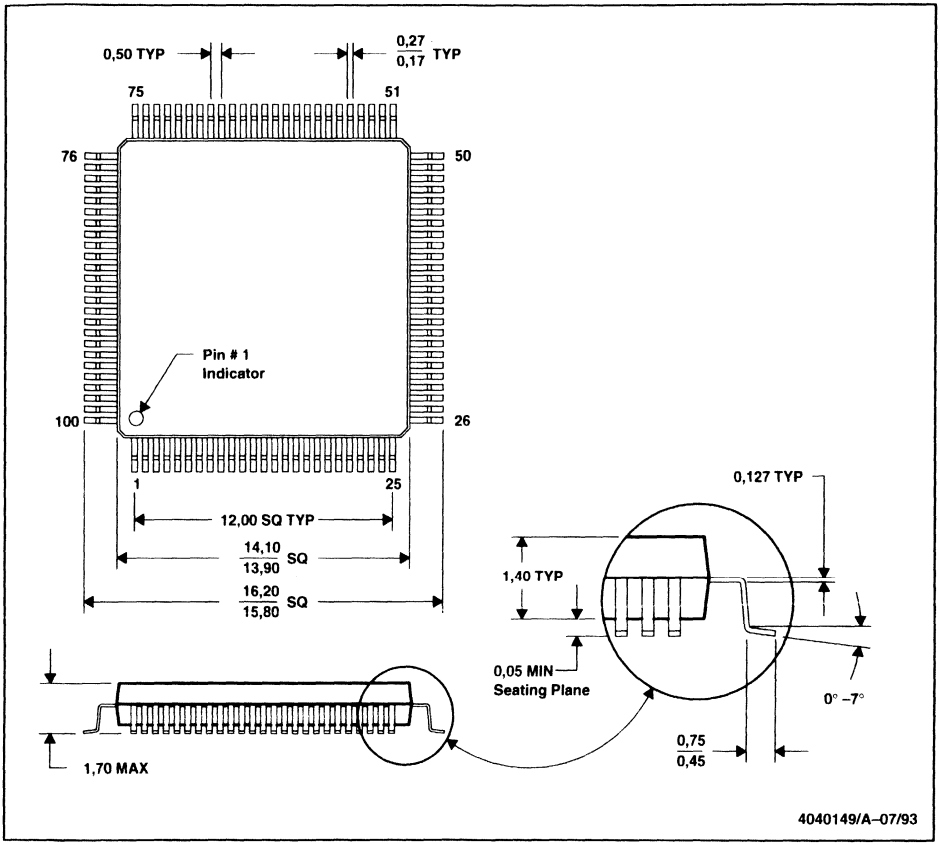
NOTES: A. Maximum deviation from coplanarity is 0,1 mm.
B. All dimensions and notes for JEDEC outline MO-xxxxx apply.

PCA100 square quad flatpack

This plastic package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperatures with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for surface mounting, and leads are spaced on 1,0-mm centers with a 0,8-mm foot length. Leads require no additional cleaning or processing when used in soldered assembly.



PZ/S-PQFP-G100 **PLASTIC QUAD FLAT PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Maximum deviation from caplanarity is 0,08 mm.

TI European Sales Offices

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Texas Instruments S.A./N.V.
Avenue Jules Bordetlaan 11
1140 Bruxelles/Brussels
Tel: (02) 7 26 75 80
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Texas Instruments GmbH
Haggertystr.1
85356 Freising
Tel: (0 81 61) 80-0 od. Nbst.
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Texas Instruments
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HOLLAND

Texas Instruments B.V.
Amsterdamseweg 204
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Tel: (020) 5 46 98 00
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HUNGARY

TI Representation
Budaörsi u. 50, 3rd floor
1112 Budapest
Tel: (1) 2 09 22 11
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EIRE

Texas Instruments Ltd.
7/8 Harcourt Street
Dublin 2
Tel: (01) 4 75 52 33
Fax: (01) 4 78 14 63

SUOMI/FINLAND

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Tekniikantie 12
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Isafjordsgatan 7
164 93 Kista
Tel: (08) 7 52 58 00
Fax: (08) 7 51 97 15

UNITED KINGDOM

Texas Instruments Ltd.
800 Pavilion Drive
Northampton Business Park,
Northampton NN47YL
Tel: (01604) 663000
Fax: (01604) 663001
Technical Enquiry Service
Tel: 0033-130 70 11 65

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English:	**(+33) 130 70 11 65**
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E-mail/Internet: *epic @ msg.ti.com
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