# Advanced Backplane Circuits Data Book



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ETL Enhanced Transceiver Logic	1
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Texas Instruments has developed Enhanced Transceiver Logic (ETL) devices designated ABTE that are compatible with the ETL standard. By using these devices, the performance and functionality of VME and proprietary TTL backplanes can be improved. Fully backward compatible with TTL, the ETL transceivers offer a narrower switching region, improved noise margins, live insertion, bushold on inputs, series damping resistors on high-drive outputs, and space-saving package options.

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Supports the VME64 ETL Specification     Reduced, TTL-Compatible, Input Threshold Range	SN54ABTE16245 WD PACKAGE SN74ABTE16245 DGG OR DL PACKAGE (TOP VIEW)				
<ul> <li>High-Drive Outputs (I<sub>OH</sub> = -60 mA, I<sub>OL</sub> = 90 mA) Support 25-Ω Incident-Wave Switching</li> </ul>	1DIR 1 48 V <sub>CC</sub> BIAS 1B1 2 47 1A1 2B1 0 3 46 2A1				
<ul> <li>V<sub>CC</sub>BIAS Pin Minimizes Signal Distortion During Live Insertion</li> </ul>	GND 0 4 45 0 GND 1B2 0 5 44 0 1A2				
<ul> <li>Internal Pullup Resistor on OE Keeps</li> <li>Outputs in High-Impedance State During</li> <li>Power Up or Power Down</li> </ul>	2B2 <b>[</b> 6 43 <b>]</b> 2A2 V <sub>CC</sub> <b>[</b> 7 42 <b>]</b> V <sub>CC</sub> 1B3 <b>[</b> 8 41 <b>]</b> 1A3				
<ul> <li>Members of the Texas Instruments</li> <li>Widebus™ Family</li> </ul>	2B3 0 9 40 0 2A3 GND 0 10 39 0 GND				
<ul> <li>State-of-the-Art EPIC-IIB<sup>TM</sup> BiCMOS Design Significantly Reduces Power Dissipation</li> </ul>	1B4 [] 11 38 [] 1A4 2B4 [] 12 37 [] 2A4 1B5 [] 13 36 [] 1A5				
<ul> <li>Distributed V<sub>CC</sub> and GND Pin Configuration</li> <li>Minimizes High-Speed Switching Noise</li> </ul>	2B5 0 14 35 0 2A5 GND 0 15 34 0 GND				
<ul> <li>25-Ω Series Dampening Resistor on B Port</li> </ul>	1B6 <b>[</b> ] 16 33 <b>[</b> ] 1A6				
<ul> <li>Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors</li> </ul>	2B6				
Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink	1B7 0 19 30 0 1A7 2B7 0 29 0 2A7				
Small-Outline (DGG) Packages and 380-Mil Fine-Pitch Ceramic Flat (WD) Package	GND   21				
Using 25-mil Center-to-Center Spacings	2DIR 24 25 OE				

#### description

The 'ABTE16245 are 16-bit (dual-octal) noninverting 3-state transceivers designed for synchronous two-way communication between data buses. The control function implementation minimizes external timing requirements. These devices can be used as two 8-bit transceivers or one 16-bit transceiver. They allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable  $(\overline{OE})$  input can be used to disable the device so that the buses are effectively isolated.

The B port has a 25- $\Omega$  series output resistor to reduce ringing. Active bus-hold inputs are also found on the B port to hold unused or floating inputs at a valid logic level.

The A port provides for the precharging of the outputs via  $V_{CC}BIAS$ , which establishes a voltage between 1.3 V and 1.7 V when  $V_{CC}$  is not connected.

The SN74ABTE16245 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABTE16245 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74ABTE16245 is characterized for operation from  $-40^{\circ}$ C to  $85^{\circ}$ C.

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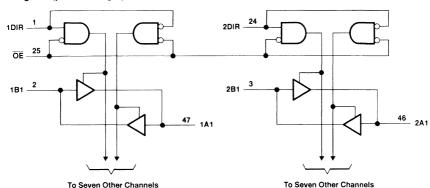


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#### FUNCTION TABLE (each 8-bit section)

INP	UTS	OPERATION
OE	DIR	OPERATION
L	L	A data to B bus
L	Н	B data to A bus
Н	X	Isolation

#### logic diagram (positive logic)



# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)	
Voltage range applied to any output in the high state or power	-off state, $V_O$ $-0.5$ V to 5.5 V
Current into any output in the low state, IO	128 mA
Input clamp current, $I_{ K }(V_1 < 0)$	10 IIIA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	–50 mA
Maximum power dissipation at $T_A = 55^{\circ}$ C (in still air) (see Note	e 2): DGG package 0.85 W
	DL package 1.2 W
Storage temperature range	65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.



The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology
 Data Book, literature number SCBD002B.

# SN54ABTE16245, SN74ABTE16245 16-BIT INCIDENT-WAVE SWITCHING BUS TRANSCEIVERS WITH 3-STATE OUTPUTS SCBS226D - JULY 1993 - REVISED AUGUST 1994

## recommended operating conditions (see Note 3)

			SN54	ABTE1	6245	SN74ABTE16245			
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
VCC	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V	High-level input voltage	ŌĒ	2			2			V
VIH	riigh-leverinput voitage	Except OE	1.6			1.6			\ \
V	Low level input veltage	ŌĒ			0.8			0.8	V
VIL	Low-level input voltage	Except OE			1.4			1.4	V
VĮ.	Input voltage		0		vcc	0		VCC	٧
1	High-level output current	B bus			-12			- 12	^
lОН	riigh-level output current	A bus			-24			-60	mA
lo.	Low-level output current	B bus			12			12	mA
IOL	Low-lever output current	A bus	T		64			90	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled			10			10	ns/V
TA	Operating free-air temperature		- 55		125	-40		85	°C

NOTE 3: Unused or floating pins (input or A-bus I/O) must be held high or low.



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# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			SN5	4ABTE1	6245	SN74ABTE16245			UNIT
			IESI CONDITIONS		MIN	TYPT	MAX	MIN	TYP	MAX	UNII
VIK		$V_{CC} = 4.5 \text{ V},$	I <sub>I</sub> = -18 mA				-1.2			-1.2	V
		$V_{CC} = 5.5 \text{ V},$	I <sub>OH</sub> = - 100 μA			V	CC-0.2		٧	CC-0.2	
	B port	VCC = 4.5 V	IOH = - 1 mA		2.4			2.4			
.,	ĺ	VCC = 4.5 V	I <sub>OH</sub> = - 12 mA		2			2			v
VOH		V <sub>CC</sub> ≈ 5.5 V,	I <sub>OH</sub> = - 1 mA				4.5			4.5	ľ
	A port	V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = - 32 mA		2.4	_		2.4			
		vCC = 4.5 v	I <sub>OH</sub> = - 64 mA					2			
	B port	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 1 mA				0.4			0.4	
\/ - ·	B port	VCC = 4.5 V	I <sub>OL</sub> = 12 mA							0.8	v
VOL		VCC = 4.5 V	IOL = 64 mA				0.55			0.55	ľ
	A port	VCC = 4.5 V	I <sub>OL</sub> = 90 mA							0.9	
		V 45V	V <sub>I</sub> = 0.8 V		100			100			
l(hold)	B port	V <sub>CC</sub> = 4.5 V	V <sub>1</sub> = 2 V		-100			-100			μΑ
		V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 0 to 5.5 V				±500			±500	
	Control inputs	$V_{CC} = 5.5 \text{ V},$	V <sub>I</sub> = V <sub>CC</sub> or GND				±1			±1	μА
l)	A or B ports	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = V <sub>CC</sub> or GND				±20			±20	μΑ .
lozh‡	A port	$V_{CC} = 5.5 \text{ V},$	V <sub>O</sub> = 2.7 V				10			10	μА
lozL‡	A port	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V				-10			-10	μА
	A port	V 55V	V- 0		-50	-120	-180	-50		-180	μΑ
Ю	B port	V <sub>CC</sub> = 5.5 V,	ΛΟ = 0		-25	-52	-90	-25		-90	μΑ
loff		V <sub>CC</sub> = 0, V <sub>CC</sub> BIAS = 0	$V_I$ or $V_O \le 4.5 \text{ V}$ ,				±100			±100	μА
				Outputs high		28	36		28	36	
loo	A or B ports	$V_{CC} = 5.5 \text{ V},$		Outputs low		38	48		38	48	mA
lcc	A or B ports	VI = V <sub>CC</sub> or GNE	ND	Outputs disabled		20	32		20	32	111/4
	D A or B ports $V_{CC} = 5 \text{ V}$ , $C_L = 50 \text{ pF}$	0 50-5	OE high		0.02			0.02		mA/	
ICCD		CL = 50 pF	OE low		0.33			0.33		MHz	
Ci	Control inputs	V <sub>I</sub> = 2.5 V or 0.	5 V			2.5	4		2.5	4	pF
Cio	I/O ports	V <sub>O</sub> = 2.5 V or 0	0.5 V			4.5	8		4.5	8	pF

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.



<sup>‡</sup> The parameters IOZH and IOZL include the input leakage current.

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### live-insertion specifications over recommended operating free-air temperature range

PARAMETER		TEST COMPLETIONS		SN54ABTE16245			SN7	11117			
		"	EST CONDITIONS	MIN	MIN TYPT		MIN	TYPT	MAX	UNIT	
		$V_{CC} = 0 \text{ to } 4.5 \text{ V},$ $I_{O(DC)} = 0$	$V_{CC}BIAS = 4.5 V \text{ to } 5.5 V,$		250	700		250	700		
ICC IV	(CCBIAS)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ $I_{O(DC)} = 0$	†, V <sub>CC</sub> BIAS = 4.5 V to 5.5 V,			20			20	PIA	
\/ -	A port	V <sub>CC</sub> = 0,	V <sub>CC</sub> BIAS = 4.5 V to 5.5 V	1.1	1.5	1.9	1.1	1.5	1.9	V	
v <sub>O</sub>	A port	$V_{CC} = 0$ ,	V <sub>CC</sub> BIAS = 4.75 V to 5.25 V	1.3	1.5	1.7	1.3	1.5	1.7	ľ	
Ю	A port	$V_{CC} = 0$ , $V_{O} = 0$	V <sub>CC</sub> BIAS = 4.5 V	-20		- 100	-20		- 100		
	^ port	$V_{CC} = 0$ , $V_{O} = 3$	V, V <sub>CC</sub> BIAS = 4.5 V	20		100	20		100	μА	

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

# switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)		V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		SN54ABTE16245		SN74ABTE16245		UNIT		
	(NAPOT)	(001701)	MIN	TYP	MAX	MIN	MAX	MIN	MAX		
<sup>†</sup> PLH	А	В	1.5	3.3	4.2	1.5	5.4	1.5	5.2	ns	
<sup>†</sup> PHL	^	В	1.5	3.8	4.6	1.5	5.4	1.5	5.2	115	
<sup>†</sup> PLH	В	А	1.5	3	3.8	1.5	4.7	1.5	4.5		
<sup>†</sup> PHL	ь	^	1.5	3.1	4	1.5	4.7	1.5	4.5	ns	
<sup>t</sup> PZH	ör.	OE	А	2	3.9	5.3	2	6.4	2	6.2	ns
<sup>†</sup> PZL	OE .	^	2	4.4	5.9	2	7	2	6.8	115	
<sup>†</sup> PZH	OĒ	В	2	4.5	6	2	7.3	2	7.1	ns	
†PZL	OE .		2	5	6.4	2	7.5	2	7.3	115	
<sup>†</sup> PHZ	ŌĒ	А	2	4.9	5.9	2	7	2	6.7		
1PLZ	OE	^	2	3.7	4.6	2	5.4	2	5.1	ns	
<sup>†</sup> PHZ	ŌĒ	В	2	5.2	6.2	2	7.2	2	7		
†PLZ	OL.	U	2	4	5	2	5.8	2	5.5	ns	



<sup>‡</sup> V<sub>CC</sub> - 0.5 V < V<sub>CC</sub>BIAS

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# extended switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Note 4 and Figure 2)

PARAMETER	FROM	TO	LOAD		CC = 5 V 4 = 25°C		SN54AB	TE16245	SN74AB	TE16245	UNIT
	(INPUT)	(OUTPUT)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
tPLH	В	А	R <sub>X</sub> = 13 Ω	1.5	3.2	4	1.5	5	1.5	4.8	ns
t <sub>PHL</sub>	В	_ ^	HX = 13.22	1.5	3.8	4.7	1.5	5.8	1.5	5.6	""
t <sub>PLH</sub>	В	А	R <sub>X</sub> = 26 Ω	1.5	3.1	4	1.5	4.8	1.5	4.6	ns
tPHL	В	_ ^	MX = 2032	1.5	3.5	4.4	1.5	5.2	1.5	4.9	2
tPLH	В	А	D. 56.0	1.5	3	3.8	1.5	4.7	1.5	4.5	ns
tPHL	В	^	R <sub>X</sub> = 56 Ω	1.5	3.3	4.2	1.5	5.1	1.5	4.7	115
	В	Α	R <sub>X</sub> = Open		0.1	0.6		2		2	
t <sub>sk(p)</sub>	Α	В			0.4	8.0		2		2	ns
	В	Α	Rχ = 26 Ω		0.3	8.0		2	L	2	
	В	А	R <sub>X</sub> = Open		0.3	0.7		1.3		1.3	
tsk(o)	Α	В			0.7	1.1		1.3		1.3	ns
( )	В	Α	$R_X = 26 \Omega$		0.5	1	1	1.3		1.3	
t <sub>t</sub> †	В	Α	Rχ = 26 Ω	0.5	0.8	1.5	0.5	1.5	0.5	1.5	ns
t <sub>t</sub> ‡	А	В	Rise or fall time 10%-90%	3.5	5.5	7.3	3.5	8.1	3.5	7.9	ns

 $t_r/t_f$  between  $V_O = 1 V/2 V$ 

# extended output characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (see Note 4 and Figures 1 and 2)

	FROM	то	TEST CONDITIONS	LOAD	SN54ABTE16245	SN74ABTE16245		UNIT
PARAMETER	(INPUT)	(OUTPUT)	TEST CONDITIONS	LOAD	MIN MAX	MIN	MAX	UNII
	Α	В	V <sub>CC</sub> = Constant,		3		2.5	
<sup>t</sup> sk(temp)	В	А	ΔT <sub>A</sub> = 20°C	Rχ = 56 Ω	4.5		4	ns
<sup>t</sup> sk(load)	В	В	V <sub>CC</sub> = Constant, Temperature = Constant	$R_X = 13, 26,$ or $56 \Omega$	4.5		4	ns

NOTE 4: Limits are specified but not tested.

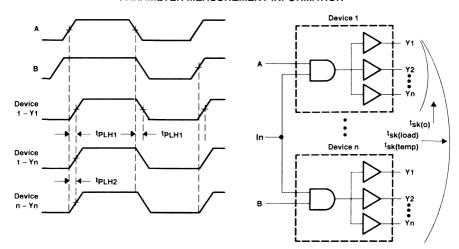


<sup>‡</sup>t<sub>r</sub>/t<sub>f</sub> between 10% and 90% of output waveform

NOTE 4: Limits are specified but not tested.

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#### PARAMETER MEASUREMENT INFORMATION



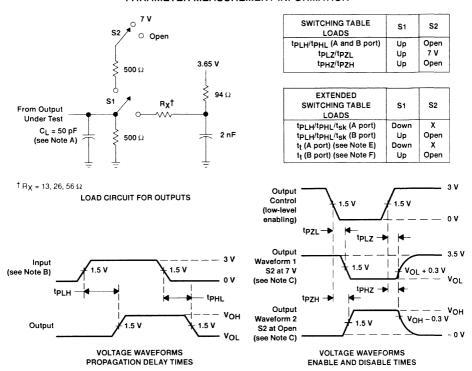
- NOTES: A. Pulse skew,  $t_{Sk(p)}$ , is defined as the difference in propagation delay times  $t_{PLH1}$  and  $t_{PHL1}$  on the same terminal at identical operating conditions.
  - B. Output skew, t<sub>sk(0)</sub>, is defined as the difference in propagation delay of the fastest and slowest paths on a single device that originate at either a single input or multiple simultaneously switched inputs, (e.g., !tpLH1 tpLH2!).
  - C. Temperature skew, tsk(temp), is the output skew of two devices, both having the same value of V<sub>CC</sub> ±1% and with package temperature differences of 20°C from each other.
  - D. Load skew,  $t_{sk(load)}$ , is measured with Rx in Figure 2 at 13  $\Omega$  for one unit and 56  $\Omega$  for the other unit

Figure 1. Voltage Waveforms for Extended Characteristics



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#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_f \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tt is measured at 1 V to 2 V.
- F. t<sub>t</sub> is measured at 10% to 90%

Figure 2. Load Circuit and Voltage Waveforms

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- Supports the VME64 ETL Specification
- Reduced, TTL-Compatible, Input Threshold Range
- High-Drive Outputs (I<sub>OH</sub> = −60 mA, I<sub>OL</sub> = 90 mA) Support 25-Ω Incident-Wave Switching
- V<sub>CC</sub>BIAS Pin Minimizes Signal Distortion During Live Insertion
- Internal Pullup Resistor on OE Keeps
   Outputs in High-Impedance State During
   Power Up or Power Down
- Members of the Texas Instruments Widebus™ Family
- State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- 25-Ω Series Dampening Resistor on B Port
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-Mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

#### SN54ABTE16246 . . . WD PACKAGE SN74ABTE16246 . . . DGG OR DL PACKAGE (TOP VIEW)

		_	1
11OEA	, –	48	V <sub>CC</sub> BIAS
11DIR [	2	47	11A
11B	3	46	10DIR
GND [	4		GND
10B	5	44	10A
9В 🛚			] 9A
v <sub>cc</sub> [	7	42	V <sub>CC</sub>
8BI <b>[</b>	8	41	9DIR
8BO <b>[</b>	9		] 8A
GND [	10		GND
7BO 🕻	11		] 7A
6BI <b>[</b>			] 7BI
6BO <b>[</b>			] 6A
5BO 🛭			] 5A
GND [		34	GND
4BO 🛭			] 5BI
4BI 🛛		32	] 4A
v <sub>cc</sub> [	18	31	v <sub>cc</sub>
3BO 🛚	19	30	<b>J</b> 3A
2BI 🛛			] 3BI
GND [			GND
2BO 🛭			] 2A
1BO 🛭		26	] 1A
1BI	24	25	OE

#### description

The "ABTE16246 are 11-bit noninverting transceivers designed for synchronous two-way communication between buses. These devices consist of open-collector and 3-state outputs. They allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable  $(\overline{OE})$  input can be used to disable the device so that the buses are effectively isolated. When  $\overline{OE}$  is low, the device is active.

The B port has a 25- $\Omega$  series output resistor to reduce ringing. Active bus-hold inputs are also found on the B port to hold unused or floating inputs at a valid logic level.

The A port provides for the precharging of the outputs via  $V_{CC}BIAS$ , which establishes a voltage between 1.3 V and 1.7 V when  $V_{CC}$  is not connected.

The SN74ABTE16246 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABTE16246 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74ABTE16246 is characterized for operation from  $-40^{\circ}$ C to 85°C.

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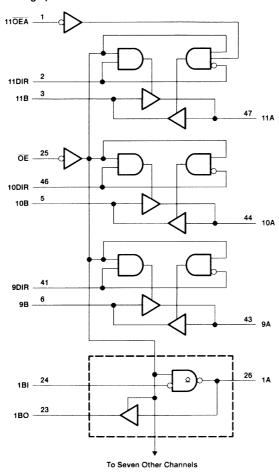


# SN54ABTE16246, SN74ABTE16246 11-BIT INCIDENT-WAVE SWITCHING BUS TRANSCEIVERS WITH 3-STATE AND OPEN-COLLECTOR OUTPUTS SCBS227B - JULY 1993 - REVISED AUGUST 1994

F١	IN	CI	TIO.	N	TA	B	F

INP	UTS	OPERATION
ŌĒ	DIR	OPERATION
L	L	A data to B bus
L	н	B data to A bus
н	X	Isolation

### logic diagram (positive logic)





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# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)	
Voltage range applied to any output in the high state or power-off state, VO	
Current into any output in the low state, IO	128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–18 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	50 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air) (see Note 2): DGG package	0.85 W
DL package	1.2 W
Storage temperature range	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
  - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
     For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

#### recommended operating conditions (see Note 3)

			SN54	ABTE1	5246	SN74	ABTE1	246	
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
VCC	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
	High-level input voltage	OE	2			2			,,
VIH	riigh-level input voltage	Except OE	1.6			1.6			V
V	Low-level input voltage	ŌĒ			0.8			0.8	V
VIL	Low-level input voltage	Except OE			1.4			1.4	V
۷он	High-level output voltage	1A-8A			5.5	0		5.5	٧
VĮ	Input voltage		0		VCC	0		VCC	٧
lo	High level output ourrent	B bus			-12			- 12	
ЮН	High-level output current	9A-11A			-24			-64	mA
lo.	Law level output ourrent	B bus			12			12	
IOL	Low-level output current	A bus			64			90	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled			10			10	ns/V
TA	Operating free-air temperature		-55	***************************************	125	-40		85	°C

NOTE 3: Unused or floating pins (input or A-bus I/O) must be held high or low.



# SN54ABTE16246, SN74ABTE16246 11-BIT INCIDENT-WAVE SWITCHING BUS TRANSCEIVERS WITH 3-STATE AND OPEN-COLLECTOR OUTPUTS SCBS227B - JULY 1993 - REVISED AUGUST 1994

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

		1	FCT CONDITIONS		SN5	4ABTE1	6246	SN7	4ABTE1	6246	UNIT
PA	RAMETER	l '	TEST CONDITIONS	•	MIN	TYPT	MAX	MIN	TYPT	MAX	UNIT
VIK		V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA				-1.2			-1.2	V
		V <sub>CC</sub> = 5.5 V,	I <sub>OH</sub> = - 100 μA			V	CC-0.2		V	CC-0.2	
	B port	V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = - 1 mA		2.4			2.4			
M -		VCC = 4.5 V	I <sub>OH</sub> = - 12 mA		2			2			V
VOH		V <sub>CC</sub> = 5.5 V,	I <sub>OH</sub> = - 1 mA				4.5			4.5	· ·
	9A11A	V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = - 32 mA		2.4			2.4			
		VCC = 4.5 V	I <sub>OH</sub> = - 64 mA					2			
ЮН	1A-8A	V <sub>CC</sub> = 4.5 V,	V <sub>OH</sub> = 5.5 V				20			20	μА
	Door	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 1 mA				0.4			0.4	
.,	B port	VCC = 4.5 V	I <sub>OL</sub> = 12 mA							0.8	v
VOL		V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 64 mA				0.55			0.55	· ·
	A port	VCC = 4.5 V	I <sub>OL</sub> = 90 mA							0.9	
		V 45V	V <sub>I</sub> = 0.8 V		100			100			
l(hold)	B port	· · · · · · · · · · · · · · · · · · ·	V <sub>I</sub> = 2 V		-100			-100			μА
		$V_{CC} = 5.5 V$ ,	$V_1 = 0 \text{ to } 5.5 \text{ V}$				±500			±500	
1.	Control inputs	Voc EEV	VI = VCC or GND	`			±1			±1	μА
4	A or B ports	VCC = 5.5 V,	Λ1 = ΛCC or GIAE	,			±20			±20	μΛ
lozh‡	9A-11A	$V_{CC} = 5.5 \text{ V},$	V <sub>O</sub> = 2.7 V				10			10	μА
loz <sub>L</sub> ‡	9A-11A	$V_{CC} = 5.5 \text{ V},$	V <sub>O</sub> = 0.5 V				-10			-10	μА
lo.	A port	V <sub>CC</sub> = 5.5 V,	Vo - 0		-50	-120	- 180	-50		-180	μА
0	B port	VCC = 3.5 V,	V() = 0		-25	-52	-90	-25		-90	μ/,
loff		$V_{CC} = 0,$ $V_{CC}BIAS = 0$	$V_I$ or $V_O \le 4.5 V$ ,				±100			±100	μА
				Outputs high		28	36		28	36	
lcc	A or B ports	V <sub>CC</sub> = 5.5 V,	IO = 0,	Outputs low		38	48		38	48	mA
	A of B ports	V <sub>I</sub> = V <sub>CC</sub> or GI	ND	Outputs disabled		20	32		20	32	111/2
		J. 5.V	0 50-5	ŌĒ high		0.02			0.02		mA/
ICCD	A or B ports	$V_{CC} = 5 V$ ,	CL = 50 pF	OE low		0.33			0.33		MHz
Ci	Control inputs	V <sub>I</sub> = 2.5 V or 0.	5 V	-		2.5	4		2.5	4	pF
Cio	I/O ports	V <sub>O</sub> = 2.5 V or 0	).5 V			4.5	8		4.5	8	pF
											·

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.



<sup>‡</sup> The parameters IOZH and IOZL include the input leakage current.

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### live-insertion specifications over recommended operating free-air temperature range

DAD	AMETER	1	TEST	CONDITIONS	SN54	ABTE1	5246	SN74	ABTE1	5246	UNIT
FAR	AWEIEN		1531	CONDITIONS	MIN	TYPT	MAX	MIN	TYPT	MAX	
ICC (VCCBIAS)		$V_{CC} = 0 \text{ to } 4$ $I_{O(DC)} = 0$	1.5 V,	V <sub>CC</sub> BIAS = 4.5 V to 5.5 V,		250	700		250	700	
		V <sub>CC</sub> = 4.5 V I <sub>O(DC)</sub> = 0	to 5.5 V <sup>‡</sup> ,	V <sub>CC</sub> BIAS = 4.5 V to 5.5 V,		20				20	μА
Vo	A port	VCC = 0,		V <sub>CC</sub> BIAS = 4.5 V to 5.5 V	1.1	1.5	1.9	1.1	1.5	1.9	.,
VO	V <sub>O</sub> A port	V <sub>CC</sub> = 0,		V <sub>CC</sub> BIAS = 4.75 V to 5.25 V	1.3	1.5	1.7	1.3	1.5	1.7	V
lo	A port	VCC = 0,	VO = 0,	V <sub>CC</sub> BIAS = 4.5 V	-20		- 100	-20		- 100	
Ю	To bou	VCC = 0,	V <sub>O</sub> = 3 V,	3 V, V <sub>CC</sub> BIAS = 4.5 V			100	20		100	μA I

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

#### switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		CC = 5 V 4 = 25°C		SN54AB	TE16246	SN74ABTE16246		UNIT
	(1147-01)	(001701)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	1
<sup>†</sup> PLH	Α	В	1.5	3.1	4.2	1.5	5.4	1.5	5.2	
tPHL	^		1.5	3.5	4.6	1.5	5.4	1.5	5.2	ns
<sup>t</sup> PLH	9B-11B	9A-11A	1.5	3	3.8	1.5	4.7	1.5	4.5	
tPHL	36-116	30-110	1.5	3.2	4	1.5	4.7	1.5	4.5	ns
t <sub>PLH</sub> §			1.5	3.2	4	1.5	4.7	1.5	4.5	ns
<sup>†</sup> PLH <sup>¶</sup>	1B-8B	1A-8A	7.5	8.9	9.7	7.5	10.6	7.5	10.3	ns
<sup>t</sup> PHL			1.5	3.2	4	1.5	4.7	1.5	4.5	ns
<sup>t</sup> PZH	ŌĒ	9A-11A	2	4.3	5.3	2	6.4	2	6.2	
†PZL	OE .	1A-11A	2	4.4	5.4	2	7	2	6.8	ns
<sup>†</sup> PZH	ŌĒ	В	2	4.3	6	2	7.3	2	7.1	
<sup>†</sup> PZL	OE.		2	4.5	6.4	2	7.5	2	7.3	ns
t <sub>PHZ</sub>	ōĒ.	9A-11A	2	4.2	5.9	2	7	2	6.7	
†PLZ	ŌĒ	1A-11A	2	3.5	4.6	2	5.4	2	5.1	ns
<sup>t</sup> PHZ	ŌĒ	В	2.5	4.3	6.2	2.5	7.2	2.5	7	
t <sub>PLZ</sub>	OL .		2	3.6	5	2	5.8	2	5.5	ns



<sup>\$</sup>VCC - 0.5 V < VCCBIAS

 $<sup>\</sup>S$  Measurement point is  $V_{OL}$  + 0.3 V.  $\P$  Measurement point is  $V_{OL}$  + 1.5 V.

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## extended switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Note 4 and Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD		CC = 5 V 4 = 25°C		SN54AB	TE16246	SN74AB	TE16246	UNIT
	(INFOT)	(OUIFUI)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
tPLH	9B-11B	9A-11A	Rχ = 13 Ω	1.5	3.2	4	1.5	5	1.5	4.8	ns
tPHL	90-110	34-114	11X = 13.22	1.5	3.8	4.7	1.5	5.8	1.5	5.6	113
tPHL	1B-8B	1A-8A	Rχ = 13 Ω	1.5	3.3	4.2	1.5	5	1.5	4.8	ns
tpLH	9B-11B	9A-11A	R <sub>X</sub> = 26 Ω	1.5	3.1	4	1.5	4.8	1.5	4.6	
tPHL	98-116	JA-IIA	HX = 5072	1.5	3.5	4.4	1.5	5.2	1.5	4.9	ns
tPHL	1B-8B	1A-8A	Rχ = 26 Ω	1.5	3.1	4	1.5	4.6	1.5	4.4	ns
<sup>t</sup> PLH	9B-11B	14 84	D., 56.0	1.5	3	3.8	1.5	4.7	1.5	4.5	ns
<sup>†</sup> PHL	90-110	1A-8A	R <sub>X</sub> = 56 Ω	1.5	3.3	4.2	1.5	5.1	1.5	4.7	115
tPHL	1B-8B	1A-8A	Rχ = 56 Ω	1.5	3	4	1.5	4.6	1.5	4.4	ns
	В	Α	R <sub>X</sub> = Open		0.1	0.6		2		2	
<sup>t</sup> sk(p)	Α	В			0.4	0.8		2		2	ns
""	В	A	$R_X = 26 \Omega$		0.3	8.0		2		2	
	В	Α	R <sub>X</sub> = Open		0.3	0.7		1.3		1.3	
<sup>t</sup> sk(o)	Α	В			0.7	1.1		1.3		1.3	ns
- (-,	B A	Α	R <sub>X</sub> = 26 Ω		0.5	1		1.3		1.3	
t <sub>t</sub> †	В	Α	$R_X = 26 \Omega$	0.5	0.8	1.5	0.5	1.5	0.5	1.5	ns
t <sub>l</sub> ‡	Α	В	Rise or fall time 10%-90%	3.5	5.5	7.3	3.5	8.1	3.5	7.9	ns

### extended output characteristics over recommended ranges of supply voltage and operating free-air temperature, C<sub>L</sub> = 50 pF (see Note 4 and Figures 1 and 2)

PARAMETER	FROM	то	TEST CONDITIONS	LOAD	SN54ABTE16246		SN74AB	UNIT	
PARAMETER	(INPUT)	(OUTPUT)	TEST CONDITIONS	LOAD	MIN	MAX	MIN	MAX	UNIT
	Α	В	V <sub>CC</sub> = Constant,			3		2.5	
<sup>t</sup> sk(temp)	В	Α	ΔT <sub>A</sub> = 20°C	Rχ = 56 Ω		4.5		4	ns
<sup>t</sup> sk(load)	В	Α	V <sub>CC</sub> = Constant, Temperature = Constant	$R_X = 13, 26,$ or $56 \Omega$		4.5		4	ns

NOTE 4: Limits are specified but not tested.

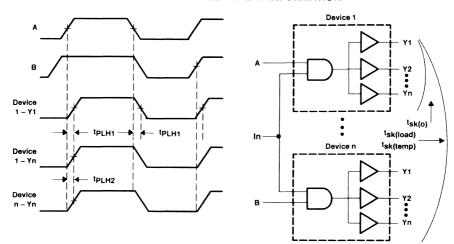


 $t_f/t_f$  between  $V_O = 1 V/2 V$ .  $t_f/t_f$  between 10% and 90% of output waveform

NOTE 4: Limits are specified but not tested.

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### PARAMETER MEASUREMENT INFORMATION



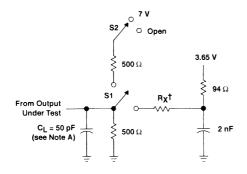
- NOTES: A. Pulse skew, t<sub>sk(p)</sub>, is defined as the difference in propagation delay times t<sub>PLH1</sub> and t<sub>PHL1</sub> on the same terminal at identical operating conditions.
  - B. Output skew, t<sub>sk(0)</sub>, is defined as the difference in propagation delay of the fastest and slowest paths on a single device that originate at either a single input or multiple simultaneously switched inputs, (e.g., Itp<sub>LH1</sub> tp<sub>LH2</sub>I).
  - C. Temperature skew, t<sub>sk(temp)</sub>, is the output skew of two devices, both having the same value of V<sub>CC</sub> ± 1% and with package temperature differences of 20°C from each other.
  - D. Load skew,  $t_{sk(load)}$ , is measured with Rx in Figure 2 at 13  $\Omega$  for one unit and 56  $\Omega$  for the other unit.

Figure 1. Voltage Waveforms for Extended Characteristics



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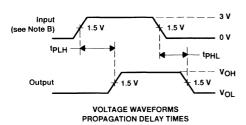
#### PARAMETER MEASUREMENT INFORMATION

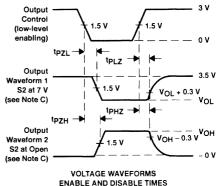


SWITCHING TABLE LOADS	S1	S2
tpLH/tpHL (9A - 11A and B port)	Up	Open
tpLH/tpHL (1A - 8A)	Up	7 V
tPLZ/tPZL	Up	7 V
tpHZ/tpZH (except 1A - 8A)	Up	Open

EXTENDED SWITCHING TABLE LOADS	S1	S2
tpLH/tpHL/tsk (A port)	Down	X
tpLH/tpHL/tsk (B port)	Up	Open
tt (A port) (see Note E)	Down	X
tt (B port) (see Note F)	Up	Open

† R<sub>X</sub> = 13, 26, 56  $\Omega$ 





NOTES: A. C<sub>1</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50~\Omega$ ,  $t_f \leq 2.5~ns$ ,  $t_f \leq 2.5~ns$ .
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t<sub>t</sub> is measured at 1 V to 2 V.
- F. tt is measured at 10% to 90%.

Figure 2. Load Circuit and Voltage Waveforms



ETL Enhanced Transceiver Logic	1
BTL Backplane Transceiver Logic	2
GTL Gunning Transceiver Logic	3
ABT/CBT 25- $\Omega$ Incident-Wave Switching Drivers	4
Mechanical Data	5

The demand for high-performance Backplane Transceiver Logic (BTL) and Futurebus+ (FB+) bus-interface devices continues to grow in telecommunications, networking, and mainframe applications. The BTL/FB+ standard uses a greatly reduced output swing and a tighter switching margin compared to the TTL standard.

The reduced-output BTL/FB+ transceivers from TI provide high drive and speed while minimizing skew and ground-bounce noise, and are compatible with IEEE 1194.1-1991 (BTL) and IEEE 896.2-1991 (FB+).

# NEXT GENERATION FUTUREBUS+/BTL TRANSCEIVERS ALLOW SINGLE-SIDED SMT MANUFACTURING

#### INTRODUCTION

Futurebus+ (IEEE 896.2-1991) and BTL (IEEE 1194.1-1991) designs offer significant performance advantages over conventional TTL backplane implementations, but these advantages come with trade-offs. Switching noise in the form of ground bounce and EMI must be controlled, and proper termination schemes must be employed to ensure signal integrity in this high speed switching environment. Trade-offs for price in the form of total system solution vs. overall system performance are also of concern. This paper begins with the historical perspective on signal integrity issues addressed by the above cited IEEE bodies, and follows with new pioneering bus interface solutions to help reduce overall FB+ or BTL system costs and design complexities.

#### CURRENT GENERATION OF FB+/BTL TRANSCEIVERS

Pursuant to the above cited IEEE standards, a number of suppliers have developed BTL and/or Futurebus+ compliant transceiver solutions. These devices share the same reduced output swing and tight switching thresholds shown in Figure 1, and also include slew rate control circuitry as shown in Figure 2. The various devices differ considerably in wafer fab process technology, propagation delay performance, and other performance metrics (Table I).

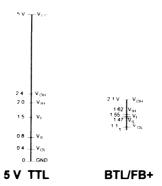


Fig. 1: Comparison of TTL and BTL switching standards

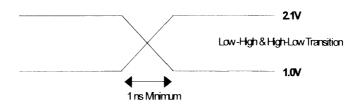


Fig 2: Illustration of Output Edge rate Control (OEC<sup>IM</sup>)

**Table I:** BTL/Futurebus+ transceiver offering on available today

Transceiver	Technology	Bits/Pkg	Tpd
ALS056/057 ®	3μ Bipolar	4/8	20ns
DS3890 ⊗	2μ Bipolar	8*	15ns
DS3896/7 ⊗	1.5µ Bipolar	4/8	12ns
DS3893A ⊗	1.2µ Bipolar	4	7ns
FB2031/40	0.8μ BiCMOS	8/9	6ns

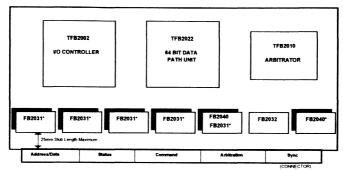
\* Note: unidirectional driver only; not a true bi-directional transceiver

® Note: not a TI product

The above table shows an evolutionary progression in bipolar wafer fab technology and hence faster propagation delay performance. Bipolar fab technologies are chosen for this class of device for their high drive capability, low switching noise, and relative ease of designing (relative to pure CMOS) the pseudo-analog circuitry required to meet the slew rate control requirement mentioned above. Bipolar circuits have the disadvantage of relatively high power dissipation. The heat generated by this high power dissipation coupled with the large switching currents coming from the bus termination place a thermal limitation on the number of bits that can be integrated into a single standard IC package (typically only 4 bits).

The newer class of BiCMOS transceivers employ a bipolar output structure to achieve the desired drive, noise, and slew rate control of the previous generation products. They also offer higher performance, much lower power dissipation, and take the next step towards higher integration (8 or 9 bits). However, even this level of density and performance is not totally sufficient for some emerging 128-bit applications. And at 9 bits, the devices are again up against the thermal capabilities of the packages; even with low power BiCMOS technology.

Futurebus+ (IEEE 896.2-1991) adds an additional constraint to board layout by mandating that all compliant cards have a maximum stub length of 25mm to reduce loading and minimize reflections. This is also a wise "rule of thumb" for non-Futurebus+ BTL designs. As data paths have increased in width from 32 to 64-bits (128-bits in the future), this stub length requirement has forced system designers to wrestle with the manufacturing problems of double-sided surface mounting of the transceivers on boards as large as 12 Standard Units (12SU). Even with the relatively dense packaging of today's fastest and most integrated transceivers, this can be a formidable design problem; adding significantly to the overall manufacturing cost of a board (Figure 3).



\* Note: the "\*" or second part type descriptor indicates that a second transceiver is mounted on the opposite side of the board

Fig 3: Uncached 64-bit FB+ layout with TI's controller chipset and today's most integrated transceivers

Another problem with the current generation of transceivers is the purchasing requirement for multiple transceiver types. Continuing with the above example, the common 64-bit uncached solution requires three different transceiver types for a complete distributed arbitration Futurebus+ implementation shown in Table II below.

**Table II:** Transceiver descriptions for 64-bit uncached FB+ board using FB20xx series transceivers

Device	Description	Qty/Board
FB2031	9-Bit Data/Address Xcver w/ Clk & Latch	9
FB2032*	Arbitration Contest Transceiver	1
FB2040	8-bit status/sync Xcver w/split TTL I/O	3
	TOTAL PART COUNT:	13

\* Optional; for distributed arbitration only

These transceivers were designed quite differently from one another due to the specific functions they perform in the system (data/address, sync, arbitration, status, or command). Figure 4 highlights the functional differences between the FB2040 (status and sync transceiver) and the FB2031 (address/data transceiver). The main distinctions to note here are the "universal" storage modes (transparent, latched, or clocked) of the FB2031 and the separate or "split" TTL I/O pins of the FB2040. And as noted above, until recently, efforts to develop any sort of true universal FB+/BTL transceiver have not been practical due to the absence of a viable high-power fine pitch package beyond 56 pins in the industry.

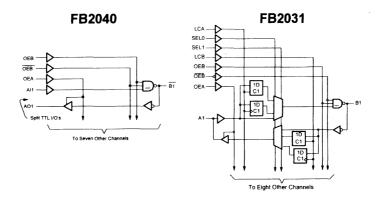


Fig 4: Functional differences between FB2040 control transceiver and FB2031 address/data transceiver

#### A NEW GENERATION OF FB+/BTL TRANSCEIVERS

As a response to the market need for single-sided surface mounting and simplified transceiver architectures, TI has developed both a high-power package and a series of 18-channel FB+/BTL Universal Bus Transceivers (UBT<sup>TM</sup>). These new devices, designated as FB16xxx series, are packaged in a high-power version of the EIAJ standard 100-pin TQFP package (0.5mm lead pitch). A package cross section is shown in figure 5 which reveals a metal heat sink that facilitates the excellent thermal performance of the package.

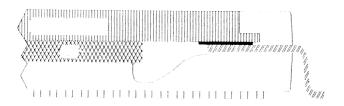


Fig 5: Cross section of thermally enhanced EIAJ 100 TQFP

The FB16xxx series devices are designed with both the universal data storage capabilities of the FB2031 address/data transceiver and the separate TTL I/O of the FB2040 control transceiver, and can be configured as two independent 9-channel or one coherent 18-channel transceiver (figure 6).

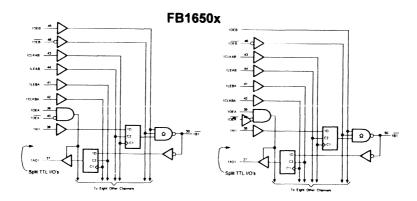
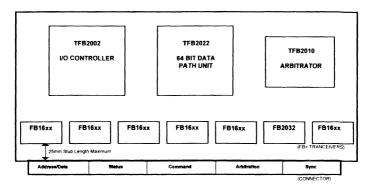


Fig 6: Functional circuit diagram of FB1650x

This flexible design approach eliminates the need for double-sided surface mounting--along with all of the associated manufacturing costs--and still meets the IEEE 896.2-1991 25mm maximum stub length requirements as shown in Figure 7.



\* Note: no double sided SMT requirement

Fig 7: Uncached 64-bit FB+ layout with TI chipset and FB16xxx transceivers

In addition, the 18 channel architecture lends itself naturally to reduced pin to pin signal skew, and advanced BiCMOS circuit design techniques have been employed to improve propagation delay performance over the previous generation of BiCMOS transceivers. Table III offers a transceiver component count comparison for the same 64-bit uncached Futurebus+ example considered previously.

**Table III:** Component count comparison for 64-bit uncached FB+ board using FB16xxx series transceivers

Device	Description	Qty/Board
FB16xxx	18-bit TTL/BTL UBT w/split TTL I/O	6
FB2032*	Arbitration Contest Transceiver	1
	TOTAL PART COUNT:	7

\* Optional; for distributed arbitration only

This represents nearly a 50% reduction in component count and a cost savings of ca. 14% on the transceivers alone. Significant savings (tens of dollars per board) on manufacturing costs are also realized by moving to single-sided SMT manufacturing. Other members of the FB16xxx family include system clock distribution features that lend themselves to more specific end system applications such as ATM hubs and routers (Table IV):

Table IV: Transceiver descriptions for other members of FB16xxx series

Device	Description		
FB1650x	18-bit TTL/BTL UBT w/split TTL I/O		
FB1651x	17-Channel UBT w/ Separate Buffered and Delayed Clk Bit		
FB1652x	17-Channel UBT w/ Separate Buffered Clk Bit (No Delay Line)		

#### CONCLUSION

The high speed data communication requirements of today's fastest board level computers and telecommunications and network switching equipments can be met with Futurebus+ and BTL compatible transceivers and switching levels. Stub length constraints and ever increasing data path widths have made it difficult to control signal integrity and manufacturing and procurement costs in these high performance systems. The next generation of 18-channel FB+/BTL Universal Bus Transceivers meets this market need by facilitating low cost single-sided surface mount manufacturing, and single-device type procurement, characterization, qualification, and specification.



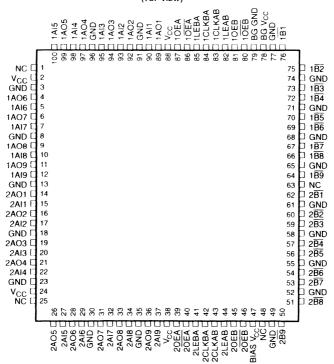
### SN54FB1650, SN74FB1650 18-BIT TTL/BTL UNIVERSAL STORAGE TRANSCIEVERS

SCBS178D - AUGUST 1992 - REVISED JULY 1995

- Compatible With IEEE 1194.1-1991 (BTL) Standard
- TTL A Port, Backplane Transceiver Logic B Port
- Open-Collector B-Port Outputs Sink 100 mA
- Isolated Logic-Ground and Bus-Ground Pins Reduce Noise
- BIAS V<sub>CC</sub> Minimizes Signal Distortion During Live Insertion/Withdrawal

- B-Port Biasing Network Preconditions the Connector and PC Trace to the Backplane Transceiver Logic High-Level Voltage
- TTL Input Structures Incorporate Active Clamping to Aid in Line Termination
- Package Options Include High-Power Shrink Quad Flat (PCA) Package With 0.5-mm Pin Pitch and Ceramic Quad Flat (HQA) Package

SN54FB1650 . . . HQA PACKAGE SN74FB1650 . . . PCA PACKAGE (TOP VIEW)



NC - No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



# SN54FB1650, SN74FB1650 18-BIT TTL/BTL UNIVERSAL STORAGE TRANSCIEVERS

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#### description

The 'FB1650 contain two 9-bit transceivers designed to translate signals between TTL and backplane transceiver logic (BTL) environments. They are specifically designed to be compatible with the IEEE 1194.1-1 (BTL) standard.

The  $\overline{B}$  port operates at BTL-signal levels. The open-collector  $\overline{B}$  ports are specified to sink 100 mA. Two output enables (OEB and  $\overline{OEB}$ ) are provided for the  $\overline{B}$  outputs. When OEB is low,  $\overline{OEB}$  is high, or  $V_{CC}$  is typically less than 2.5 V, the  $\overline{B}$  port is turned off.

The A port operates at TTL-signal levels. The A outputs reflect the inverse of the data at the  $\overline{B}$  port when the A-port output enable (OEA) is high. When OEA is low or when  $V_{CC}$  is typically less than 2.5 V, the A outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating TTL inputs at a valid logic state.

BIAS  $V_{CC}$  establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when  $V_{CC}$  is not connected.

BG V<sub>CC</sub> and BG GND are the supply inputs for the bias generator.

The SN54FB1650 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74FB1650 is characterized for operation from 0°C to 70°C.

# Function Tables

#### TRANSCEIVER

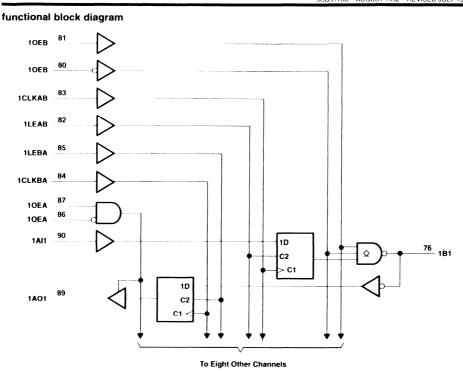
	INP	UTS		FUNCTION	
OEA	OEA	OEB	OEB	FUNCTION	
×	Х	Н	L	A data to B bus	
L	н	×	×	B data to A bus	
L	Н	Н	L	A data to B bus, B data to A bus	
X	Х	L	Х	B-bus isolation	
×	X	X	н	B-ous isolation	
Н	Х	Х	Х	A-bus isolation	
Х	L	Х	Х	A-bus isolation	

#### STORAGE MODE

INP	UTS	FUNCTION	
LE	CLK		
Н	X	Transparent	
L	1	Store data	
L	L	Storage	



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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub> , BIAS V <sub>CC</sub> , BG V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> : except $\overline{B}$ port	
B̄ port	1.2 V to 3.5 V
Voltage range applied to any $\overline{B}$ output in the disabled or power-off state, $V_O$	. −0.5 V to 5.5 V
Voltage range applied to any output in the high state, V <sub>O</sub>	0.5 V to V <sub>CC</sub>
Input current range (except B port)	
Current applied to any single output in the low state, I <sub>O</sub> : A port	48 mA
B̄ port	200 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air) (see Note 1): PCA package	1.8 W
Storage temperature range, T <sub>stq</sub>	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 75 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.



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## recommended operating conditions (see Note 2)

			SN	54FB16	50	SN	74FB16	50	UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	UNII
V <sub>CC</sub> , BG V <sub>CC</sub>	Supply voltage		4.5	5	5.5	4.5	5	5.5	٧
BIAS VCC	Supply voltage		4.5	5	5.5	4.5	5	5.5	٧
	10.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.	B port	1.62		2.3	1.62		2.3	v
VIH	High-level input voltage	Except B port	2		Ų.	2			l
		B port	0.75	<i>A</i>	1.47	0.75		1.47	v
V <sub>IL</sub>	Low-level input voltage	Except B port		7	0.8			0.8	·
lik	Input clamp current			S	-18			-18	mA
ЮН	High-level output current	A port	- 6	8	-3			-3	mA
		A port	Q.		24			24	mA
OL	Low-level output current	B̄ port			100			100	ША
<sup>T</sup> A	Operating free-air temperature		-55		125	0		70	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

### electrical characteristics over recommended operating free-air temperature range

DADAMETED		7507.00	TEST CONDITIONS		54FB16	50	SN	50	UNIT	
	PARAMETER	TEST CO	DIDITIONS	MIN	TYP	MAX	MIN	TYPT	MAX	UNIT
	B port	45.4	I <sub>I</sub> = -18 mA			-1.2			-1.2	v
VIK	Except B port	V <sub>CC</sub> = 4.5 V	I <sub>I</sub> = -40 mA			-0.5			~0.5	,
.,	AO port	V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = -1 mA							V
VOH	AO port	VCC = 4.5 V	$I_{OH} = -3 \text{ mA}$	2.5	3.3		2.5	3.3		
	AO port	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 24 mA		0.35	0.5		0.35	0.5	
VOL	- ·	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 80 mA	0.75		1.1	0.75		1.1	V
	B port	VCC = 4.5 V	I <sub>OL</sub> = 100 mA			1.15			1.15	
lį.	Except B port	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 5.5 V			50			50	μΑ
ηн‡	Except B port	$V_{CC} = 5.5 \text{ V}$	V <sub>I</sub> = 2.7 V		THE STATE OF THE S	<b>3</b> 50			50	μA
. +	Except B port	$V_{CC} = 5.5 \text{ V},$	$V_1 = 0.5 V$		Š	-50			-50	μA
IIL‡	B port	V <sub>CC</sub> = 5.5 V,	V <sub>1</sub> = 0.75 V		S. S.	-100			-100	μΛ
lozh	AO port	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V		Ŝ	50			50	μA
lozL	AO port	$V_{CC} = 5.5 \text{ V},$	V <sub>O</sub> = 0.5 V	<u> </u>	<u>Š</u> _	-50			-50	μA
lozpu	AO port	$V_{CC} = 0 \text{ to } 2.1 \text{ V},$	$V_O = 0.5 \text{ to } 2.7 \text{ V}$		5	50			50	μА
IOZPD	AO port	$V_{CC} = 2.1 \text{ V to } 0$ ,	$V_O = 0.5 \text{ to } 2.7 \text{ V}$	Q`		-50			-50	μА
ЮН	B port	$V_{CC} = 0 \text{ to } 5.5 \text{ V},$	V <sub>O</sub> = 2.1 V			100			100	μА
los§	A port	$V_{CC} = 5.5 \text{ V},$	VO = 0	- 30		-150	- 30		-150	mA
laa	A port to B port	V <sub>CC</sub> = 5.5 V,	IO = 0			100			100	mA
lcc	B port to A port	VCC = 5.5 V,	10 = 0			120			120	
Ci	Al port	V <sub>I</sub> = V <sub>CC</sub> or GND			5.5			5.5		pF
9	Control pins	1 - ACC 01 GIAD			5.5			5.5		
Co	AO ports	$V_O = V_{CC}$ or GND			5.5			5.5		pF
C <sub>io</sub> ¶	B port per P1194.0	V <sub>CC</sub> = 0 to 5.5 V				5.5			5.5	pF

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

Parameter is based on characterization but is not tested.



<sup>‡</sup> For I/O ports, the parameters I<sub>IH</sub> and I<sub>IL</sub> include the off-state output current.

<sup>§</sup> Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second

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### live-insertion specifications over recommended operating free-air temperature range

PARAMETER			TEST CONDITIONS			SN74FI	B1650		
PAN	AMEIER		TEST CONDITIONS	MIN	MAX	MIN	MAX	UNIT	
I (D	IAS V <sub>CC</sub> )	V <sub>CC</sub> = 0 to 4.5 V	V- 04-0V V (BIACV ) 45-V4-55-V		450		450		
ICC (p	iiwa ACC)	V <sub>CC</sub> = 4.5 V to 5.5 V	$V_B = 0 \text{ to } 2 \text{ V},  V_I \text{ (BIAS V}_{CC}) = 4.5 \text{ V to } 5.5 \text{ V}$		Q 10		10	μА	
٧o	B port	V <sub>CC</sub> = 0,	V <sub>I</sub> (BIAS V <sub>CC</sub> ) = 4.5 V to 5.5 V	1.624	2.1	1.62	2.1	V	
		$V_{CC} = 0$ , $V_B = 1 V$ ,	$V_I$ (BIAS $V_{CC}$ ) = 4.5 V to 5.5 V	3		-1			
Ю	B port	V <sub>CC</sub> = 0 to 5.5 V,	OEB = 0 to 0.8 V	8	100		100	μΑ	
		V <sub>CC</sub> = 0 to 2.2 V,	OEB = 0 to 5 V	Q	100		100		

## timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25 C		= 5 V, 25 C SN54FB165		SN74FB1650		UNIT	
			MIN	MAX	MIN	MA	MIN	MAX	ĺ	
fclock	Clock frequency		0	150	0	350	0	150	MHz	
tw	Pulse duration, CLK or LE		3.3		3.3	Ser.	3.3		ns	
	Catus time	Data before LE	4.8		5.54		4.8			
t <sub>su</sub>	Setup time	Data before CLK↑	4.9		535		4.9		ns	
	I be Asil Africa	Data after LE	1.8		Q 8		1.8			
th	Hold time	Data after CLK↑	1.1		Q 1.1		1.1		ns	

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## switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

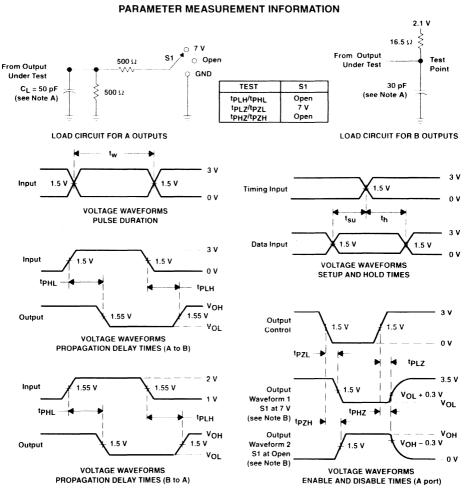
PARAMETER	FROM	TO (OUTPUT)		CC = 5 \ A = 25 C		SN54F	B1650	SN74F	B1650	UNIT
	(INPUT)	(001P01)	MIN	TYPT	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			150			150		150		MHz
t <sub>PLH</sub>	Al	B	1.8	3.7	5.3	1.8	6.6	1.8	6.2	ns
<sup>†</sup> PHL	]^	B	2.9	4.4	6	2.9	7.3	2.9	7.2	115
†PLH	LEAB	В	2.7	4.2	5.8	2.7	6.9	2.7	6.4	ns
<sup>†</sup> PHL	CEAB	В	3.5	5	6.5	3.5	7.5	3.5	7.3	13
<sup>t</sup> PLH	CLKAB	B	2.3	3.9	5.5	2.3	6.5	2.3	6	ns
<sup>†</sup> PHL	OLIVID		2.9	4.5	6.1	2.9	6.8	2.9	6.7	
<sup>t</sup> PLH	В	AO	3.5	5.9	7.9	3.5	9.7	3.5	8.6	ns
<sup>†</sup> PHL	В	AO .	2.2	3.7	5.3	2.2	6	2.2	5.7	113
t <sub>PLH</sub>	LEBA	AO	1.8	3.2	4.6	1.8	5.4	1.8	5.1	ns
<sup>†</sup> PHL	LEBA	AO	1.7	3	4.4	1.7	5.1	1.7	4.7	113
<sup>t</sup> PLH	CLKBA	AO	1.8	3.1	4.6	1.8	5.3	1.8	5.1	ns
<sup>†</sup> PHL	CLNDA	A0	1.7	3.1	4.6	1.7	€.3	1.7	4.9	110
t <sub>PLH</sub>	OEB	Ē	2.7	4.6	6.4	2.7	₹ 7.4	2.7	6.7	ns
<sup>†</sup> PHL	OEB	В	2.9	4.1	5.9	2.9	6.8	2.9	6.6	10
tpLH	ÖĒB	В	2.6	4.3	6.2	सु	7.2	2.6	6.6	ns
<sup>†</sup> PHL	OEB	В	3.4	4.6	6.4	<sub>.</sub> 2€.4	7.2	3.4	7	115
tpzH	OFA	AO	1.4	2.9	4.4	1.4	5.3	1.4	4.9	ns
t <sub>PZL</sub>	OEA	AO	.1.4	2.6	4	1.4	4.9	1.4	4.6	115
<sup>†</sup> PHZ	OFA	AO	1.7	3.4	5.1	1.7	5.9	1.7	5.8	ns
†PLZ	OEA	AO	2.2	3.6	5	2.2	5.8	2.2	5.5	
<sup>†</sup> PZH	OEA	AO	1.7	3.3	4.7	1.7	5.9	1.7	5.5	ns
<sup>†</sup> PZL	OEA	AO	1.7	3.1	4.4	1.7	5.4	1.7	5.1	115
<sup>t</sup> PHZ	OEA	AO	1.5	2.9	4.5	1.5	5.2	1.5	5.1	ns
<sup>†</sup> PLZ	OEA	Α0	2	3.1	4.6	2	5	2	4.8	113
t <sub>sk(p)</sub> ‡ Skew for any single channel∃tp⊢L – tpL⊢		Al to B or B to AO		0.5						ns
t <sub>sk(o)</sub> ‡ Skew between drivers in the same package		Al to B or B to AO		1						ns
	Transition time, B out	Transition time, B outputs (1.3 V to 1.8 V)		1.7	3.1	0.3	6.8	0.5	4.6	
tt	Transition time, AO outputs (10% to 90%)		0.5	2	3.6	0.3	4.3	0.4	4.2	ns
tPR	B-port input pulse reje	ection	1			1		1		ns

<sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25 \text{ C}$ .



<sup>‡</sup> Skew values are applicable for through mode only.

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NOTES: A. C<sub>1</sub> includes probe and jig capacitance

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: TTL inputs PRR  $\leq$  10 MHz,  $Z_Q = 50 \Omega$ ,  $t_f \leq$  2.5 ns. tf  $\leq$  2.5 ns. BTL inputs PRR  $\leq$  10 MHz,  $Z_Q = 50 \Omega$ ,  $t_f \leq$  2.5 ns. tf  $\leq$  2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

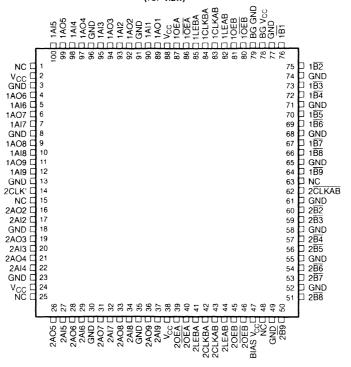




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- Compatible With IEEE 1194.1-1991 (BTL) Standard
- TTL A Port, Backplane Transceiver Logic
- Open-Collector B-Port Outputs Sink
- Isolated Logic-Ground and Bus-Ground Pins Reduce Noise
- B-Port Biasing Network Preconditions the Connector and PC Trace to the Backplane Transceiver Logic High-Level Voltage
- TTL Input Structures Incorporate Active Clamping to Aid in Line Termination
- Package Options Include High-Power Shrink Quad Flat (PCA) Package With 0.5-mm Pin Pitch and Ceramic Quad Flat (HQA) Package

SN54FB1651 . . . HQA PACKAGE SN74FB1651 . . . PCA PACKAGE (TOP VIEW)



NC - No internal connection



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#### description

The 'FB1651 contain an 8-bit and a 9-bit transceiver with a buffered clock. The clock and the transceivers are designed to translate signals between TTL and backplane transceiver logic (BTL) environments. They are specifically designed to be compatible with the IEEE 1194.1-1 (BTL) standard.

The  $\overline{B}$  port operates at BTL-signal levels. The open-collector  $\overline{B}$  ports are specified to sink 100 mA. Two output enables (OEB and  $\overline{OEB}$ ) are provided for the  $\overline{B}$  outputs. When OEB is low,  $\overline{OEB}$  is high, or  $V_{CC}$  is typically less than 2.5 V. the  $\overline{B}$  port is turned off.

The A port operates at TTL-signal levels. The A outputs reflect the inverse of the data at the  $\overline{B}$  port when the A-port output enable (OEA) is high. When OEA is low or when  $V_{CC}$  is typically less than 2.5 V, the A outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating TTL inputs at a valid logic state.

BIAS  $V_{CC}$  establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when  $V_{CC}$  is not connected.

BG V<sub>CC</sub> and BG GND are the supply inputs for the bias generator.

The SN54FB1651 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74FB1651 is characterized for operation from  $-40^{\circ}$ C to 85°C.

#### **Function Tables**

#### TRANSCEIVER

	INP	UTS		FUNCTION					
OEA	OEA	OEB	OEB	FUNCTION					
Х	×	Н	L	A data to B bus					
L	н	X	X	B data to A bus A data to B bus, B data to A bus					
L	Н	Н	L						
Х	Х	L	Х	B-bus isolation					
Х	×	X	Н	B-bus isolation					
Н	X	Х	X	A hus is eletion					
х	L	Χ	Χ	A-bus isolation					

#### STORAGE MODE

INP	UTS	FUNCTION
LE	CLK	FUNCTION
Н	Х	Transparent
L	1	Store data
L	L	Storage

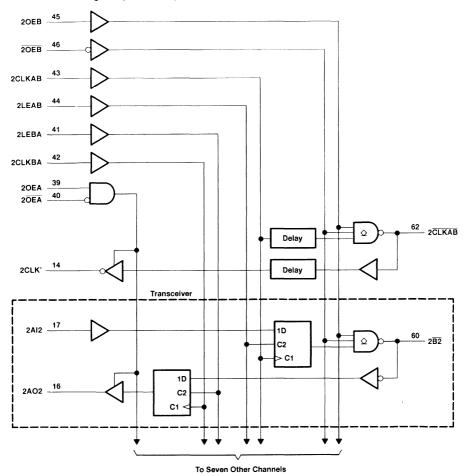


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## functional block diagram 10EB -81 10EB 80 1CLKAB 83 1LEAB 82 1LEBA 85 1CLKBA -87 10EA 10EA Transceiver 1AI1 -1D 76 1B1 C2 > C1 1D 1A01 -C2 To Eight Other Channels

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#### functional block diagram (continued)



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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub> , BIAS V <sub>CC</sub> , BG V <sub>CC</sub>
Input voltage range V: event B net
Input voltage range, V <sub>I</sub> : except B port
B port
Input current range (except B port) –40 mA to 5 mA
Voltage range applied to any $\overline{B}$ output in the disabled or power-off state0.5 V to 5.5 V
Voltage range applied to any output in the high state
Current applied to any single output in the low state: A port
B̄ port
Maximum power dissipation at $T_A = 55^{\circ}$ C (in still air) (see Note 1): PCA package
Storage temperature range, T <sub>stg</sub> –65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions (see Note 2)

			SN	SN54FB1651 SN74FB1651			UNIT		
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
V <sub>CC</sub> , BG V <sub>CC</sub>	Supply voltage		4.5	5	5.5	4.5	5	5.5	٧
BIAS VCC	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V	High-level input voltage	B̄ port	1.62		2.3	1.62		2.3	.,
V <sub>IH</sub> H		Except B port	2	Š	Ų,	2			V
V	Low-level input voltage	B port	0.75	de	1.47	0.75		1.47	V
VIL	Low-level input voltage	Except B port		Ž	0.8			0.8	V
ЧK	Input clamp current			કું	-18			-18	mA
loн	High-level output current	A port	800	5	-3			-3	mA
lo.	Low-level output current	A port	Q.		24			24	4
OL	Low-level output current	B port			100			100	mA
$T_A$	Operating free-air temperature		-55		125	-40		85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.



NOTE 1: The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 75 mils. For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, Iterature number SCBD002B.

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#### electrical characteristics over recommended operating free-air temperature range

		7507.00	NIDITIONS	SN	154FB16	51	SN	74FB16	51	UNIT
	PARAMETER	I EST CC	ONDITIONS	MIN	TYPT	MAX	MIN	TYPT	MAX	UNII
ViK		V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA			-1.2			-1.2	٧
	10	V 45V	IOH = -1 mA							V
∨он	AO port	V <sub>CC</sub> = 4.5 V	IOH = -3 mA	2.5	3.3		2.5	3.3		٧
	AO port	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 24 mA		0.35	0.5		0.35	0.5	
VOL		V <sub>CC</sub> = 4.5 V	IOL = 80 mA	0.75		1.1	0.75		1.1	V
	B port	VCC = 4.5 V	I <sub>OL</sub> = 100 mA			1.15			1.15	
11	Except B port	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 5.5 V			50			50	μΑ
IJH <sup>‡</sup>	Except B port	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 2.7 V			<b>\$</b> 50			50	μА
. +	Except B port	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 0.5 V		,	-50			-50	μА
կլ‡	B port	$V_{CC} = 5.5 \text{ V},$	V <sub>I</sub> = 0.75 V		S. S.	-100			-100	μΑ
lоzн	AO port	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V		X	50			50	μА
lozu	AO port	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V		5	-50			-50	μА
lozpu	AO port	$V_{CC} = 0 \text{ to } 2.1 \text{ V},$	V <sub>O</sub> = 0.5 to 2.7 V		3	50			50	μА
lozpd	AO port	$V_{CC} = 2.1 \text{ V to 0},$	$V_O = 0.5 \text{ to } 2.7 \text{ V}$	Q		-50			-50	μА
Iон	B port	$V_{CC} = 0 \text{ to } 5.5 \text{ V},$	V <sub>O</sub> = 2.1 V			100			100	μА
IOS§	A port	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0	- 30		-150	- 30		-150	mA
laa	A port to B port	V <sub>CC</sub> = 5.5 V,	10 = 0			100			100	mA
ICC	B port to A port	VCC = 5.5 V,	IQ = 0			120			120	IIIA
	Al port	V V = = or CND			5.5			5.5		ρF
Ci	Control pins	V <sub>I</sub> = V <sub>CC</sub> or GND			5.5			5.5		Pi
Co	AO ports	$V_O = V_{CC}$ or GND			5.5			5.5		pF
Cio	B port per P1194.0	V <sub>CC</sub> = 0 to 5.5 V				5.5			5.5	ρF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC}$  = 5 V,  $T_A$  = 25°C.

### live-insertion specifications over recommended operating free-air temperature range

DAD	AMETER	TEST CONDITIONS	TEST CONDITIONS	SN54F	B1651	SN74F	31651	UNIT
PAH	AMEIER	TEST CONDITIONS	TEST CONDITIONS	MIN	MAX	MIN	MAX	UNIT
laa /B	DIAC Vaal	V <sub>CC</sub> = 0 to 4.5 V	V <sub>B</sub> = 0 to 2 V, V <sub>I</sub> (BIAS V <sub>CC</sub> ) = 4.5 V to 5.5 V		<b>5</b> 0		450	^
LICC (E	BIAS V <sub>CC</sub> )	V <sub>CC</sub> = 4.5 V to 5.5 V			2 10		10	μА
VO	B port	V <sub>CC</sub> = 0,	V <sub>I</sub> (BIAS V <sub>CC</sub> ) = 4.5 V to 5.5 V	1.62	2.1	1.62	2.1	V
		$V_{CC} = 0$ , $V_{B} = 1 V$ ,	V <sub>I</sub> (BIAS V <sub>CC</sub> ) = 4.5 V to 5.5 V	3		-1		
10	B̄ port	$V_{CC} = 0 \text{ to } 5.5 \text{ V},$	OEB ≈ 0 to 0.8 V	,o	100		100	μΑ
		$V_{CC} = 0 \text{ to } 2.2 \text{ V},$	OEB = 0 to 5 V	Q	100		100	

<sup>‡</sup> For I/O ports, the parameters I<sub>IH</sub> and I<sub>II</sub> include the off-state output current.

<sup>9</sup> Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

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# timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			V <sub>CC</sub> :	V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		SN54FB1651		SN74FB1651		
			MIN	MAX	MIN	MAX	MIN	MAX		
<sup>1</sup> clock	Clock frequency		0	150		<b>3</b> 50		150	MHz	
tw	Pulse duration	CLK or LE	3.3		3.3	Ø.	3.3		ns	
	Cat 1:	Data before LE	4.8		5.54		4.8			
<sup>t</sup> su	Setup time	Data before CLK↑	4.9		53		4.9		ns	
	Held Co.	Data after LE	1.8	1.8			1.8			
<sup>t</sup> h	Hold time	Data after CLK↑	1.1		Q1.8 Q 1.1		1.1		ns	

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## switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	TO (OUTPUT)	7	CC = 5 \ A = 25°C	/, >	SN54F	B1651	SN74FB1651		UNIT
	(INPUT)	(OUIPUI)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			150			150		150		MHz
<sup>†</sup> PLH	Al	B	1.8	3.7	5.3	1.8	6.6	1.8	6.2	
tPHL	<b>1</b> A'	В	2.9	4.4	6	2.9	7.3	2.9	7.2	ns
t <sub>PLH</sub>	LEAB	B	2.7	4.2	5.8	2.7	6.9	2.7	6.4	
<sup>†</sup> PHL	1	В	3.5	5	6.5	3.5	7.5	3.5	7.3	ns
t <sub>PLH</sub>	CLKAB	B	2.3	3.9	5.5	2.3	6.5	2.3	6	
t <sub>PHL</sub>	CLNAB	В	2.9	4.5	6.1	2.9	6.8	2.9	6.7	ns
t <sub>PLH</sub>	2CLKAB	2CLKAB	4.6	6.9	8.8	4.6	10.7	4.6	9.9	
t <sub>PHL</sub>	ZULKAB	2CLKAB	4.9	6.5	8.1	4.9	9.2	4.9	8.8	ns
t <sub>PLH</sub>	_	40	3.5	5.9	7.9	3.5	9.7	3.5	8.6	
<sup>†</sup> PHL	B	AO	2.2	3.7	5.3	2.2	6	2.2	5.7	ns
t <sub>PLH</sub>	1504	40	1.8	3.2	4.6	1.8	5.4	1.8	5.1	ns ns
tPHL	LEBA	AO	1.7	3	4.4	1.7	5.1	1.7	4.7	
t <sub>PLH</sub>	OLIVBA	40	1.8	3.1	4.6	1.8	Ę	1.8	5.1	
t <sub>PHL</sub>	CLKBA	AO	1.7	3.1	4.6	1.7	£,5.3	1.7	4.9	
<sup>t</sup> PLH			6.4	9.7	11.8	6.4.4	<b>2</b> 15	6.4	13.4	
tPHL	2CLKBA	2CLK'	4.1	6.9	8.9	4,0	11.2	4.1	10.3	ns
<sup>t</sup> PLH		B	2.7	4.6	6.4	S)	7.4	2.7	6.7	
tPHL	OEB		2.9	4.1	5.9	2.9	6.8	2.9	6.6	ns
t <sub>PLH</sub>		B	2.6	4.3	6.2	2.6	7.2	2.6	6.6	ns
tPHL	OEB		3.4	4.6	6.4	3.4	7.2	3.4	7	
<sup>t</sup> PZH		4.0	1.4	2.9	4.4	1.4	5.3	1.4	4.9	
†PZL	OEA	AO	1.4	2.6	4	1.4	4.9	1.4	4.6	ns
tPHZ		40	1.7	3.4	5.1	1.7	5.9	1.7	5.8	
tPLZ	OEA	AO	2.2	3.6	5	2.2	5.8	2.2	5.5	ns
tPZH		4.0	1.7	3.3	4.7	1.7	5.9	1.7	5.5	
†PZL	ŌĒĀ	AO	1.7	3.1	4.4	1.7	5.4	1.7	5.1	ns
t <sub>PHZ</sub>		4.0	1.5	2.9	4.5	1.5	5.2	1.5	5.1	
t <sub>PLZ</sub>	ŌĒĀ	AO	2	3.1	4.6	2	5	2	4.8	ns
t <sub>sk(p)</sub> ‡ Skew for any single channel   tpHL - tpLH		Al to $\overline{\mathbb{B}}$ or $\overline{\mathbb{B}}$ to AO		0.5						ns
tsk(o) <sup>‡</sup> Skew between drivers in the same package		Al to $\overline{B}$ or $\overline{B}$ to AO		1						ns
tt	Transition time, B out	outs (1.3 V to 1.8 V)	0.9	1.7	3.1	0.3	6.8	0.5	4.6	ne
r	Transition time, AO outputs (10% to 90%)			2	3.6	0.3	4.3	0.4	4.2	ns
tpR	B-port input pulse reje	ection	1			1		1		ns

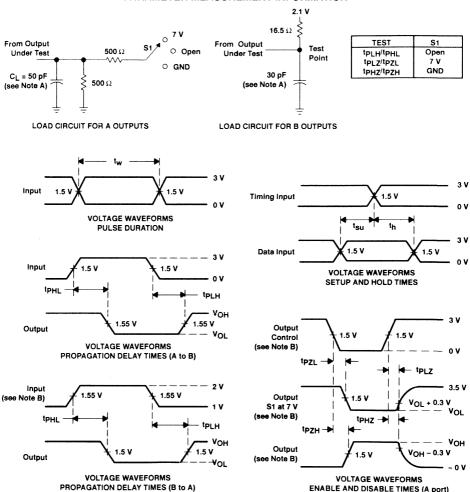
<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.



<sup>‡</sup> Skew values are applicable for through mode only.

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#### PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: TTL inputs PRR  $\leq$  10 MHz,  $Z_O$  = 50  $\Omega$ ,  $t_f \leq$  2.5 ns. BTL inputs PRR  $\leq$  10 MHz,  $Z_O$  = 50  $\Omega$ ,  $t_f \leq$  2.5 ns.  $t_f \leq$  2.5 ns.
  - D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

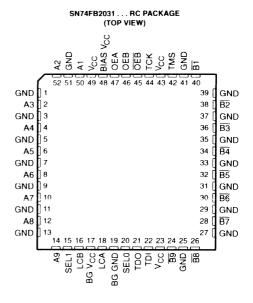




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- Compatible With IEEE 1194.1-1991 (BTL) Standard
- TTL A Port, Backplane Transceiver Logic (BTL) B Port
- Open-Collector B-Port Outputs Sink 100 mA
- Isolated Logic-Ground and Bus-Ground Pins Reduce Noise
- BIAS V<sub>CC</sub> Minimizes Signal Distortion During Live Insertion/Withdrawal
- B-Port Biasing Network Preconditions the Connector and PC Trace to the BTL High-Level Voltage
- TTL-Input Structures Incorporate Active Clamping to Aid in Line Termination
- Package Options Include Plastic Quad Flat (RC) Package and Ceramic Flat (WD) Package





#### description

The 'FB2031 are 9-bit transceivers designed to translate signals between TTL and backplane transceiver logic (BTL) environments. They are specifically designed to be compatible with IEEE 1194.1-1991 (BTL).

The  $\overline{B}$  port operates at BTL-signal levels. The open-collector  $\overline{B}$  ports are specified to sink 100 mA. Two output enables (OEB and  $\overline{OEB}$ ) are provided for the  $\overline{B}$  outputs. When OEB is low,  $\overline{OEB}$  is high, or  $V_{CC}$  is typically less than 2.5 V, the  $\overline{B}$  port is turned off.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



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#### description (continued)

The A port operates at TTL-signal levels. The A outputs reflect the inverse of the data at the  $\overline{B}$  port when the A-port output enable (OEA) is high. When OEA is low or  $V_{CC}$  is typically less than 2.5 V, the A outputs are in the high-impedance state.

Pins are allocated for the 4-wire IEEE 1149.1 (JTAG) test bus. TMS and TCK are not connected and TDI is shorted to TDO.

BIAS V<sub>CC</sub> establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when V<sub>CC</sub> is not connected.

BG V<sub>CC</sub> and BG GND are the supply inputs for the bias generator.

To ensure the high-impedance state during power up or power down, A port should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resister is determined by the current-sinking capability of the driver.

The SN54FB2031 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74FB2031 is characterized for operation from 0°C to 70°C.

#### **Function Tables**

#### TRANSCEIVER

	INPUTS		FUNCTION
OEA	OEB	ŌĒB	FUNCTION
L	Н	L	À data to B bus
H H	L X	X	B̄ data to A bus
Н	Н	L	A data to B bus, B data to A bus
L L	L X	X H	Isolation

#### STORAGE MODE

LCA, LCB	RESULT
0	Transparent
1	Latches latched
1	Flip-flops triggered

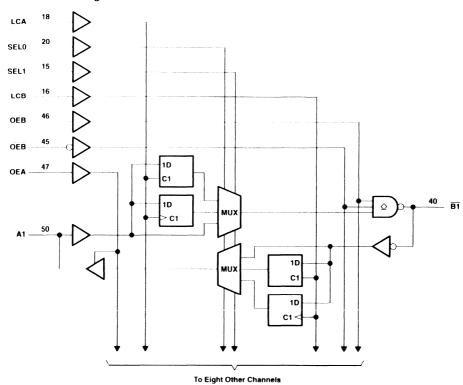
#### SELECT

SEL1	SEL0	MUX A→B	MUX B⊶A
0	0	Latch	Latch
0	1	Through	Through
1	0	Flip-flop	Flip-flop
1	1	Flip-flop	Latch



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### functional block diagram



Pin numbers shown are for the RC package

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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> : except B port	1.2 V to 7 V
$\widetilde{B}$ port	1.2 V to 3.5 V
Input clamp current: except B port	40 mA
$\overline{B}$ port	–18 mA
Voltage range applied to any B output in the disabled or power-off state	0.5 V to 5.5 V
Voltage range applied to any output in the high state	$-0.5$ V to $V_{CC}$
Current applied to any single output in the low state: A port	48 mĀ
B port	200 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air) (see Note 1): RC package	1.4 W
Storage temperature range, T <sub>stg</sub>	−65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions (see Note 2)

			SN	54FB20	31	SN74FB2031			UNIT
			MIN NOM MAX			MIN	NOM	MAX	UNIT
V <sub>CC</sub> , BIAS V <sub>CC</sub> . BG V <sub>CC</sub>	Supply voltage		4.5	5	5.5	4.5	5	5.5	٧
.,		B̄ port	1.62*	Q	2.3	1.62		2.3	v
VIII	High-level input voltage	Except B port	2	Ø.		2			ľ
	Law tarabian Arabana	B port	0.75	Q.C.	1.47*	0.75		1.47	v
VIL	Low-level input voltage	Except B port		<u>, Ĝ</u>	0.8			0.8	ľ
ЮН	High-level output current	A port	\$	37	-3			- 3	mA
		A port	,£		24			24	
OL	Low-level output current	B port	-		100			100	mA
TA	Operating free-air temperature		- 55		125	0		70	°C

<sup>\*</sup>On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not tested.

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.



NOTE 1: The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 75 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B

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## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

		T		SN	154FB20	31	SN	74FB20	31	UNIT
١ '	PARAMETER	IESI CO	NDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNII
,,	B port	45.4	l <sub>I</sub> = −18 mA			-1.2			-1.2	V
VIK	Except B port	V <sub>CC</sub> = 4.5 V	I <sub>I</sub> = -40 mA			- 0.5			-0.5	V
VOH	A port	V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> =1 mA		3.2					V
VOH	A port	VCC - 4:5 V	I <sub>OH</sub> = - 3 mA	2.5	3.3		2.5	3.3		<u> </u>
	A port	Vcc = 4.5 V	I <sub>OL</sub> = 20 mA		0.31					
VOL	Арон	AGC = 4.2 A	I <sub>OL</sub> = 24 mA	1	0.35	2.0 %		0.35	0.5	] ,
*OL	B port	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 80 mA	0.75	0 35	11	0.75		1.1	•
		VC(, - 4.5 V	I <sub>OL</sub> = 100 mA		Z.	1.15			1.15	
l <sub>l</sub>	Except B port	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 5.5 V	TO A	1	50			50	μА
I <sub>IH</sub> ‡	Except B port	V <sub>CC</sub> = 5 5 V.	V <sub>I</sub> = 2 7 V		<u>3</u>	50			50	μA
	Except B port	V <sub>CC</sub> = 5.5 V,	$V_{\parallel} = 0.5 \ V$	Q	,	~ 50			- 50	μА
IIL ‡	B port	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 0.75 V	Q		-100			- 100	,,,,, 
<sup>l</sup> ozh	A port	$V_{CC} = 2.1 \text{ V to } 5.5 \text{ V},$	V <sub>O</sub> = 2.7 V			50			50	μΑ
l <sub>OZL</sub>	A port	$V_{CC} = 2.1 \text{ V to } 5.5 \text{ V}.$	V <sub>O</sub> = 0.5 V			50			- 50	μА
lozpu	A port	$V_{CC} = 0$ to 2.1 V,	$V_0 = 0.5 \text{ V to } 2.7 \text{ V}$			50			50	μΑ
IOZPD	A port	$V_{CC} = 2.1 \text{ V to } 0$ ,	V <sub>O</sub> = 0.5 V to 2.7 V			- 50			- 50	μΑ
<sup>1</sup> ОН	B port	V <sub>CC</sub> = 0 to 5.5 V.	V <sub>O</sub> = 2.1 V			100			100	μА
los§	A port	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0	- 30		-150	- 30		-150	mA
	A port to B port	V <sub>CC</sub> = 5 5 V.	IO - 0			78			78	mA
'cc	B port to A port	ACC = 2.2 A'	10 - 0		78				78	mA
Ci		V <sub>I</sub> = 0.5 V or 2.5 V			4.5			4.5		pF
C 1	A port	V <sub>O</sub> = 0.5 V or 2.5 V			8.5			8.5		n.E
Cio <sup>11</sup>	B port per P1194.0	V <sub>CC</sub> = 0 to 5 5 V				6			6	pF

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25 C

### live-insertion specifications over recommended operating free-air temperature range

D40	AMETER		TEST CONDITIONS			SN74FB2031			
PARAMETER			TEST CONDITIONS			MIN	MAX	UNIT	
	2140.1/	V <sub>CC</sub> = 0 to 4.5 V	V <sub>B</sub> = 0 to 2 V. V <sub>I</sub> (BIAS V <sub>CC</sub> ) = 4.5 V to 5.5 V		<b>3</b> 50		450		
I CC (E	BIAS V <sub>CC</sub> )	V <sub>CC</sub> = 4.5 V to 5.5 V	VB = 0 to 2 v. V  (BIAS VCC) = 4.5 V to 5.5 V		<u>و</u> 10	10		μА	
VO	B port	V <sub>CC</sub> = 0.	VI (BIAS V <sub>CC</sub> ) = 5 V	1.62	2.1	1.62	2.1	٧	
		V <sub>CC</sub> = 0 .	$V_B = 1 \text{ V}$ , $V_I \text{ (BIAS V}_{CC}) = 4.5 \text{ V to } 5.5 \text{ V}$	30		-1			
10	B port	$V_{CC} = 0 \text{ to } 5.5 \text{ V}.$	OEB = 0 to 0.8 V	No.	100		100	μА	
		$V_{CC} = 0 \text{ to } 2.2 \text{ V}.$	OEB = 0 to 5 V	Q.	100		100		

<sup>‡</sup> For I/O ports, the parameters I<sub>IH</sub> and I<sub>IL</sub> include the off-state output current.

<sup>§</sup> Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

Parameter is based on characterization but is not tested.

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# timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		SN54	FB2031	SN74F	B2031	
		MIN	MAX	MIN	MAX	UNIT
fclock	Clock frequency	0	150	0	150	MHz
t <sub>w</sub>	Pulse duration, LCA or LCB	3.3	***	3.3		ns
	Setup time, data before LCA <sup>↑</sup> (clock mode)		Š	1.4		
	Setup time, data before LCB↑ (clock mode)	2.8	g.	2.8		
t <sub>su</sub>	Setup time, data before LCA↑ (latch mode)	1.1	4	1.1		ns
	Setup time, data before LCB↑ (latch mode)	25	,	2.4		
	Hold time, data after LCA↑ (clock mode)	<b>20</b> 6		0.6		
	Hold time, data after LCB↑ (clock mode)	Q 0		0		
th	Hold time, data after LCA↑ (latch mode)	0.9		0.9		ns
	Hold time, data after LCB↑ (latch mode)			0		

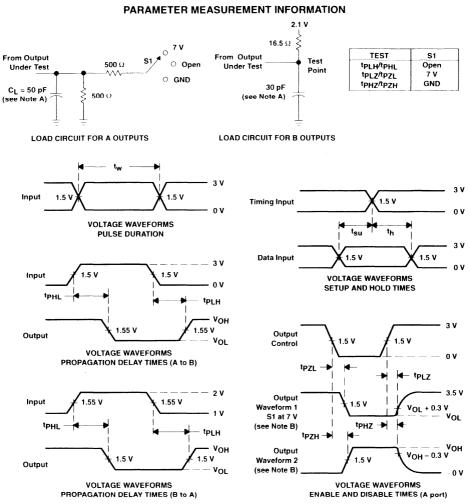


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# switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

D.	ARAMETER	FROM	то	vcc =	5 V, TA	= 25 C	SN54F	B2031	SN74F	B2031	UNIT
	ANAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
	f <sub>max</sub>					150		150		150	MHz
	<sup>†</sup> PLH	A (through mode)	B	3.7	4.5	5.9	3.2	8	3.2	6.6	
	<sup>t</sup> PHL	A (inrodgir mode)	В	2.9	4	5.7	2.6	7.8	2.6	5.9	ns
	<sup>†</sup> PLH	A (transparent)	В	4.1	5	6.5	3.6	8.6	3.6	7.3	ns
	<sup>t</sup> PHL	A (ilansparent)	В	3.3	4.5	6.1	3	8.3	3	6.5	IIS
	<sup>†</sup> PLH	LCA	В	4.5	5.4	7	3.9	9.1	3.9	7.8	ns
	<sup>†</sup> PHL	COA	В	4	5.1	6.7	3.4	9	3.4	7.4	] "
	<sup>t</sup> PLH	LCB	А	2.8	3.7	4.7	1.9	7.9	1.9	6	ns
	<sup>†</sup> PHL	1		2.5	3.4	4.9	1.8	7.4	1.8	5.5	
	<sup>†</sup> PLH	SEL1 or SEL0	А	2.5	3.8	5.3	1.9	7.9	1.9	6.3	
	<sup>†</sup> PHL	SELT OF SELO		2.2	3.5	5.1	1.6	7.1	1.6	5.6	ns
	<sup>†</sup> PLH	SEL1 or SEL0	В	4.1	5.3	6.9	3.7	<b>3</b> 3	3.7	7.8	
<sup>†</sup> PHL		SELT OF SELO	В	3.7	5.2	6.9	3.3	9.2	3.3	7.7	ns
	†PLH	D (#	А	3.1	4	5.6	22,4	8 6	2.2	7 1	ns
<sup>†</sup> PHL		B (through mode)	~	2.6	3.4	4.9	1,60	7.6	1.4	5.7	ns
<sup>†</sup> РLН †РНL †РLН		B (1	А	3.3	4.2	5.9	<b>€</b> 4	9	2.4	7.6	
		B (transparent)	^	2.8	3.9	5.5	Q 1.8	8.2	1.8	6.3	ns
		OEB or OEB	B	3.7	4.6	6.1	3.2	8.4	3.2	6.7	ns
	<sup>†</sup> PHL	OEB OLOEB	В	2.9	4.3	5.8	2.5	8.2	2.5	6.4	ns
	<sup>†</sup> PZH	OEA	А	2.3	3.1	4.5	1.6	7.3	1.6	5	ns
	<sup>†</sup> PZL			1.9	2.7	4.1	1.6	7	1.6	4.4	
	tPHZ	OEA	٨	2.2	3.1	4.5	1.5	7.1	1.5	5.2	ns
	<sup>†</sup> PLZ	OEA	Α	2.5	3.3	4.9	2	7.2	2	5.2	
<sup>†</sup> sk(p)	Skew for any single channel	А	B		0.5						ns
'SK(P)	Itpht - tpth	Ë	Α		0.3						115
	Skew between	А	В	1	0.2						
<sup>†</sup> sk(o)	drivers in the same package	B	А		0.3						ns
	Transition time, B outputs (1.3 V to 1.8 V)			0.6	2	2.8	0.3	3.3	0.4	2.9	
11	Transition time, A outputs (10% to 90%)				3.5	4.7	0	6.4	0	5.4	ns
B-port in	put pulse rejection			1			1		1		ns

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.



- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: TTL inputs PRR < 10 MHz,  $Z_O$  = 50  $\Omega$ ,  $t_f$  < 2.5 ns.  $t_f$
  - D. The outputs are measured one at a time with one transition per measurement

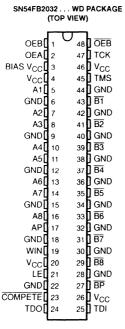
Figure 1. Load Circuits and Voltage Waveforms

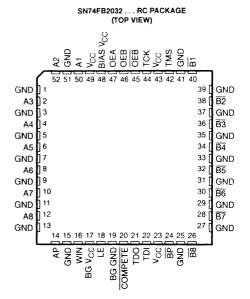


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- Compatible With IEEE 1194.1-1991 (BTL) and IEEE 896.2-1991 (Futurebus+)
- TTL A Port, Backplane Transceiver Logic
   B Port
- Open-Collector B-Port Outputs Sink 100 mA
- Minimum B-Port Edge Rate = 2 ns
- Isolated Logic-Ground and Bus-Ground Pins Reduce Noise

- BIAS V<sub>CC</sub> Pin Minimizes Signal Distortion During Live Insertion/Withdrawal
- B-Port Biasing Network Preconditions the Connector and PC Trace to the Backplane Transceiver Logic High-Level Voltage
- TTL-Input Structures Incorporate Active Clamping Networks to Aid in Line Termination
- Package Options Include Plastic Quad Flat (RC) Package and Ceramic Flat (WD) Package





#### description

The 'FB2032 are 9-bit transceivers designed to translate signals between TTL and backplane transceiver logic (BTL) environments and to perform bus arbitration. They are specifically designed to be compatible with IEEE 1194.1-1991 (BTL) and IEEE 896.2-1991 (Futurebus+) standards.

The  $\overline{B}$  port operates at BTL-signal levels. The open-collector  $\overline{B}$  ports are specified to sink 100 mA and have minimum output edge rates of 2 ns. Two output enables, OEB and  $\overline{OEB}$ , are provided for the  $\overline{B}$  outputs. When OEB is low,  $\overline{OEB}$  is high, or  $V_{CC}$  is typically less than 2.5 V, the  $\overline{B}$  port is turned off.



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#### description (continued)

The A port operates at TTL-signal levels. The A outputs reflect the inverse of the data at the  $\overline{B}$  port when the A-port output enable, OEA, is high. When OEA is low or when  $V_{CC}$  is typically less than 2.5 V, the A outputs are in the high-impedance state.

The A-port data can be latched by taking the latch enable (LE) high. When LE is low, the latches are transparent.

The Futurebus+ protocol logic can be activated by taking  $\overline{\text{COMPETE}}$  low. The module (device) then compares its A data (arbitration number) against the A data of another identical module also connected to the  $\overline{\text{B}}$  arbitration bus, and sets WIN high if the A data is greater than the A data of the other module (i.e., has higher priority). A8 and  $\overline{\text{BB}}$  are the most significant bits, and A1 and  $\overline{\text{B1}}$  are the least significant bits. If OEB is high and  $\overline{\text{OEB}}$  is low during this operation and the A bus of the first module wins priority, the A bus asserts its arbitration number on the  $\overline{\text{B-}}$ -arbitration bus.

AP and  $\overline{BP}$  are the bus-parity bits. The winning module may assert  $\overline{BP}$  low if its parity bit (AP) is high.

In a typical operating sequence, a Futurebus+ arbitration controller latches its arbitration number into the A port and waits for the results of a competition. When the competition is complete, and if the controller's arbitration number did not win, the controller reads back the current value of the  $\overline{B}$  bus (by taking OEA high) and determines the winning arbitration number. This allows the module to change its arbitration number for the next competition cycle, if desired.

Pins are allocated for the four-wire IEEE 1149.1 (JTAG) test bus, which will be implemented in a future version of the 'FB2032. Currently, TMS and TCK are not connected and TDI is shorted to TDO.

BIAS  $V_{CC}$  establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when  $V_{CC}$  is not connected.

BG V<sub>CC</sub> and BG GND are the supply inputs for the bias generator.

The SN54FB2032 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74FB2032 is characterized for operation from 0°C to 70°C.



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#### **Function Tables**

#### TRANSCEIVER

	INPUTS		5 INOTION
OEA	OEB	OEB	FUNCTION
L	Н	L	Ā data to B bus
H	L X	X H	B data to A bus
н	Н	L	Ā data to B bus, B data to A bus
L	X	Х Н	Isolation

#### WIN

	INPUTS						
OEB	OEB	COMPETE	DATA A1, A2†	WIN			
Н	Н	Х	Х	L			
Н	L	н	×	L			
Н	L	L	A1 < A2	L			
н	L	L	A2 ≤ A1	н			

† A1 refers to the A data of Module 1 and A2 refers to the A data of Module 2. If LE=L, A=current A data. If LE=H, A=the value of A8-A1 prior to the most recent low-to-high transition of LE.

#### RP

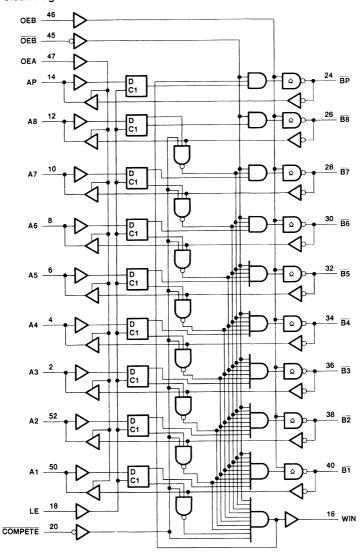
	<u> </u>								
	INPUTS								
OEB	OEB	WIN	AP‡	ВР					
L	X	Х	Х	Н					
Х	н	×	X	н					
Н	L	L	X	н					
н	L	н	L	н					
н	L	н	н	L					

† If LE=L, AP=current AP data, if LE=H, AP= the level of AP prior to the most recent low-to-high transition of LE.



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### functional block diagram



Pin numbers shown are for the RC package.



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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> : except $\overline{BP}$ , $\overline{B}$ port	1.2 V to 7 V
BP, B port	-1.2 V to 3.5 V
Input current range (except $\overline{B}$ port)	-40 mA to 5 mA
Voltage range applied to any B output in the disabled or power-off state	-0.5 V to 5.5 V
Voltage range applied to any output in the high state	0.5 V to V <sub>CC</sub>
Current applied to any single output in the low state: A port	48 mA
B port	200 mA
Maximum power dissipation at $T_A = 55$ °C (in still air) (see Note 1): RC package	1.4 W
Storage temperature range	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions (see Note 2)

			SN	54FB20	32	SN	74FB20	32	UNIT	
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
V <sub>CC</sub> , BIAS V <sub>CC</sub> , BG V <sub>CC</sub>	Supply voltage		4.5	5	5.5	4.5	5	5.5	٧	
		BP, B port	1.62		2.3	1.62		2.3	V	
V <sub>IH</sub> High-level input voltage	riigii-level input voltage	Except B port	2			2			V	
M	Low leveling duelloon	BP, B port	0.75		1.47	0.75		1.47	V	
VIL	Low-level input voltage	Except B port	1		0.8			0.8	٧	
iк	Input clamp current		1		-18			-18	mA	
ЮН	High-level output current	AP, WIN, A port	1					-3	mA	
		AP, WIN, A port						24	4	
lor	Low-level output current	BP, B port			100			100	mA	
TA	Operating free-air temperature		-55		125	0		70	°C	

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.



NOTE 1. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 75 mils. For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, Iterature number SCB0002B.

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## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

		7507.00	TEST CONDITIONS		54FB20	32	SN	UNIT		
	PARAMETER	TEST CO	TEST CONDITIONS			MIN TYPT MAX		MIN TYPT MAX		UNII
,,	BP, B port	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA			-1.2			-1.2	V
ViK	Except BP, B port	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -40 mA			-0.5			-0.5	
VOH	AP, WIN, A port	$V_{CC} = 4.5 \text{ V},$	I <sub>OH</sub> = -3 mA	2.5	3.3		2.5	3.3		V
.,	AP, WIN, A port	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 24 mA		0.35	0.5		0.35	0.5	v
VOL	BP, B port	V <sub>CC</sub> = 4.5 V,	IOL ≈ 80 mA	0.75		1.1	0.75		1,1	V
II.	Except BP, B port	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 5.5 V			50			50	μА
1 <sub>H</sub> ‡	Except BP, B port	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 2.7 V			50			50	μА
	Except BP, B port	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 0.5 V			-50			-50	
IIL‡	BP, B port	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 0.75 V	_		-100			-100	μА
ЮН	BP, B port	$V_{CC} = 0 \text{ to } 5.5 \text{ V},$	V <sub>O</sub> = 2.1 V			100			100	μА
IOS§	AP, WIN, A port	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0	- 30		-150	- 30		-150	mA
	A port to B port	V 55V	1- 0		25			25		mA
1cc	B port to A port	V <sub>CC</sub> = 5.5 V,	IO = 0		60			60		IIIA
Ci		V <sub>I</sub> = V <sub>CC</sub> or GND				5			5	pF
Co	A port	VO = VCC or GND								pF
	B nort per B1104.0	V <sub>CC</sub> = 0 to 4.5 V				6			6	pF
Cio	B port per P1194.0	V <sub>CC</sub> = 4.5 V to 5.5	V			5			5	pΓ

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

#### live-insertion specifications over recommended operating free-air temperature range

			TEGT CONDITIONS	SN54F	B2032	SN74F	B2032	
PARA	AMETER		TEST CONDITIONS	MIN	MAX	MIN	MAX	UNIT
I /DI	IAC V \	V <sub>CC</sub> = 0 to 4.5 V	V- 0400V V: (BIAC V) 4 E V to E E V		450		450	
iCC (pi	IAS V <sub>CC</sub> )	V <sub>CC</sub> = 4.5 V to 5.5 V	$V_B = 0 \text{ to } 2 \text{ V},  V_I \text{ (BIAS V}_{CC}) = 4.5 \text{ V to } 5.5 \text{ V}$		10		10	μА
ν <sub>O</sub>	B port	V <sub>CC</sub> = 0,	V <sub>I</sub> (BIAS V <sub>CC</sub> ) = 4.5 V to 5.5 V	1.62	2.1	1.62	2.1	٧
		V <sub>CC</sub> = 0,	V <sub>B</sub> = 1 V, V <sub>I</sub> (BIAS V <sub>CC</sub> ) = 4.5 V to 5.5 V	-1		-1		
Ю	B port	$V_{CC} = 0 \text{ to } 5.5 \text{ V},$	OEB = 0 to 0.8 V		100		100	μΑ
		V <sub>CC</sub> = 0 to 2.2 V,	OEB = 0 to 5 V		100		100	

<sup>‡</sup> For I/O ports, the parameters I<sub>IH</sub> and I<sub>IL</sub> include the off-state output current.

<sup>9</sup> Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

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# switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC =	= 5 V, 25°C	SN54F	B2032	SN74F	B2032	UNIT
	(INFOT)	(001201)	MIN	MAX	MIN	MAX	MIN	MAX	l
<sup>t</sup> PLH	A or AP	B or BP				8		8	ns
<sup>t</sup> PHL	A OI AI	BOIDE				8		8	113
<sup>t</sup> PLH	A					9		9	ns
<sup>t</sup> PHL	^	B <sub>n - 1</sub>				9		9	115
<sup>t</sup> PLH	A	ВР				10		10	ne
<sup>t</sup> PHL	^	BP				10		10	ns
<sup>†</sup> PLH	B	5				9		9	ns
<sup>t</sup> PHL	В	B̄ <sub>n − 1</sub>				9		9	115
<sup>t</sup> PLH	LE	Ē				7.5		7.5	ns
<sup>t</sup> PHL		В				7.5		7.5	115
<sup>t</sup> PLH	LE	BP				7.5		7.5	
<sup>†</sup> PHL		BP				7.5		7.5	ns
<sup>t</sup> PLH	B or BP	A or AP				7.5		7.5	
<sup>t</sup> PHL	B or BP	A OF AP				7.5		7.5	ns
tPLH	5	1401				8.5		8.5	
tPHL	B	WIN				8.5		8.5	ns
<sup>t</sup> PLH						7.6		7.6	ns
tPHL	- A	WIN				7.6		7.6	
tPLH						7		7	
<sup>t</sup> PHL	LE	WIN				7		7	ns
†PLH						5.5		5.5	
tPHL	COMPETE	WIN				5.5		5.5	ns
<sup>t</sup> PLH						6	-	6	
tPHL	ŌĒB	WIN				6		6	ns
<sup>†</sup> PLH		=				7.5		7.5	
<sup>t</sup> PHL	COMPETE	B				7.5		7.5	ns
<sup>t</sup> PLH	COLUMNIE					6.5		6.5	
tpHL	COMPETÉ	BP				6.5		6.5	ns
<sup>†</sup> PLH	055	-				6.5	•	6.5	
<sup>†</sup> PHL	OEB	B				6.5		6.5	ns
<sup>†</sup> PLH	055	5				6.5		6.5	
<sup>†</sup> PHL	ŌĒB	B				6.5		6.5	ns
<sup>t</sup> PZH	054		1			5.5		5.5	
tPZL	OEA	A				5.5		5.5	ns
<sup>†</sup> PHZ	054					7		7	
tPLZ	OEA	A				7		7	ns
tţ	Transition time, B outputs	1.3 V to 1.8 V)	2		1	3	1	3	ns
tPR	B-port input pulse rejection					1		1	ns



#### PARAMETER MEASUREMENT INFORMATION **16.5** Ω TEST S1 From Output From Output Test **500** Ω Open tPLH/tPHL **Under Test Under Test** Point 7 V tPLZ/tPZL O GND tPHZ/tPZH GND 30 pF C<sub>1</sub> = 50 pF 500 Ω (see Note A) (see Note A) LOAD CIRCUIT FOR A OUTPUTS LOAD CIRCUIT FOR B OUTPUTS 3 V Input 1.5 V 1.5 V Timing Input **VOLTAGE WAVEFORMS** t<sub>su</sub> PULSE DURATION 3 V 15 V Data Input 1.5 V 0 V Input **VOLTAGE WAVEFORMS** (see Note B) SETUP AND HOLD TIMES <sup>t</sup>PLH Vон 3 V 1 55 V 1.55 V Output Output VOL Control **VOLTAGE WAVEFORMS** (see Note B) PROPAGATION DELAY TIMES (A to B) <sup>t</sup>PZL - tplz 3.5 V Input 1.55 V 1.55 V Output (see Note B) V<sub>OL</sub> + 0.3 V S1 at 7 V VOL (see Note C) tpHZ → **TPHL** tpzH → VOH VOH Output V<sub>OH</sub> - 0.3 V Output (see Note C)

NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

**VOLTAGE WAVEFORMS** 

PROPAGATION DELAY TIMES (B to A)

B. All input pulses are supplied by generators having the following characteristics: TTL inputs – PRR  $\leq$  10 MHz,  $Z_O \approx 50 \Omega$ ,  $t_f \leq 2.5$  ns.  $t_f \leq 2.5$  ns. BTL inputs – PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_f \leq 2.5$  ns.  $t_f \leq 2.5$  ns.

VOLTAGE WAVEFORMS

ENABLE AND DISABLE TIMES (A port)

- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

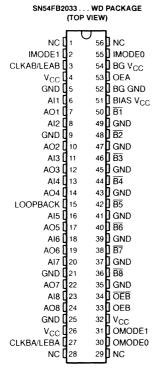
Figure 1. Load Circuits and Voltage Waveforms



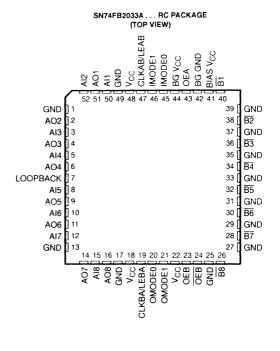
### SN54FB2033, SN74FB2033A 8-BIT TTL/BTL REGISTERED TRANSCEIVERS

SCBS174D - NOVEMBER 1991 - REVISED JULY 1994

- TTL A Port, Backplane Transceiver Logic (BTL) B Port
- Open-Collector B-Port Outputs Sink 100 mA
- Isolated Logic-Ground and Bus-Ground Pins Reduce Noise
- BIAS V<sub>CC</sub> Pin Minimizes Signal Distortion During Live Insertion/Withdrawal
- B-Port Biasing Network Preconditions the Connector and PC Trace to the Backplane Transceiver Logic High-Level Voltage
- TTL-Input Structures Incorporate Active Clamping Networks to Aid in Line Termination
- Package Options Include Plastic Quad Flat (RC) Package and Ceramic Flat (WD) Package









## SN54FB2033, SN74FB2033A 8-BIT TTL/BTL REGISTERED TRANSCEIVERS

SCBS174D - NOVEMBER 1991 - REVISED JULY 1994

#### description

The SN54FB2033 and SN74FB2033A are 8-bit transceivers featuring a split input (Al) and output (AO) bus on the TTL-level A port. The common-I/O, open-collector  $\overline{B}$  port operates at backplane transceiver logic (BTL) signal levels.

The logic element for data flow in each direction is configured by two mode inputs (IMODE1 and IMODE0 for B-to-A, OMODE1 and OMODE0 for A-to-B) as a buffer, a D-type flip-flop, or a D-type latch. When configured in the buffer mode, the inverted input data appears at the output port. In the flip-flop mode, data is stored on the rising edge of the appropriate clock input (CLKAB/LEAB or CLKBA/LEBA). In the latch mode, the clock pins serve as active-high transparent latch enables.

Data flow in the B-to-A direction, regardless of the logic element selected, is further controlled by the LOOPBACK input. When LOOPBACK is low,  $\overline{B}$ -port data is the B-to-A input. When LOOPBACK is high, the output of the selected A-to-B logic element (prior to inversion) is the B-to-A input.

The AO port-enable/-disable control is provided by OEA. When OEA is low or when V<sub>CC</sub> is less than 2.5 V, the AO port is in the high-impedance state. When OEA is high, the AO port is active (high or low logic levels).

The  $\overline{B}$  port is controlled by OEB and  $\overline{OEB}$ . If OEB is low,  $\overline{OEB}$  is high, or  $V_{CC}$  is less than 2.5 V, the  $\overline{B}$  port is inactive. If OEB is high and  $\overline{OEB}$  is low, the B port is active.

BG V<sub>CC</sub> and BG GND are the bias-generator reference inputs.

The A-to-B and B-to-A logic elements are active regardless of the state of their associated outputs. The logic elements can enter new data (in flip-flop and latch modes) or retain previously stored data while the associated outputs are in the high-impedance (AO port) or inactive ( $\overline{B}$  port) states.

Output clamps are provided on the BTL outputs to reduce switching noise. One clamp reduces inductive ringing effects on  $V_{OH}$  during a low-to-high transition. The other clamps out ringing below the BTL  $V_{OL}$  voltage of 0.75 V. Both these clamps are active only during AC switching and do not affect the BTL outputs during steady-state conditions.

BIAS V<sub>CC</sub> establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when V<sub>CC</sub> is not connected.

The SN54FB2033 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74FB2033A is characterized for operation from 0°C to 70°C.



## SN54FB2033, SN74FB2033A 8-BIT TTL/BTL REGISTERED TRANSCEIVERS

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#### **Function Tables**

#### FUNCTION/MODE TABLE

				INPUTS				FUNCTION/MODE
OEA	OEB	OEB	OMODE1	OMODE0	IMODE1	IMODE0	LOOPBACK	FUNCTION/MODE
L	L	Х	Х	Х	Х	Х	×	Isolation
L	X	Н	X	X	X	Х	X	isolation
Х	Н	L	L	L	Х	Х	×	Al to B, buffer mode
Х	Н	L	l.	Н	Х	Х	X	Al to B, flip-flop mode
Х	Н	L	Н	Х	X	X	Х	Al to B, latch mode
Н	L	Х	Х	Х	L	L	L	540
Н	Χ	Н	Х	X	L	L	L	B to AO, buffer mode
Н	L	Х	Х	X	L	Н	L	E. 40 # #
Н	×	Н	X	X	L	н	L	B to AO, flip-flop mode
Н	L	Х	Х	Х	Н	X	L	ï. •0
Н	X	Н	Х	X	Н	X	L	B to AO, latch mode
Н	L	Х	X	Х	L	L	Н	A14- A0 b #
Н	×	н	X	X	L	L	н	Al to AO, buffer mode
Н	L	Х	Х	Х	L	Н	Н	411. 40 (1) (1)
Н	X	Н	X	X	L	н	н	Al to AO, flip-flop mode
Н	L	Х	Х	Х	Н	Х	Н	
Н	Х	Н	Х	Х	Н	X	н	Al to AO, latch mode
Н	Н	L	X	Х	X	Х	L	Al to B, B to AO



## **Function Tables (Continued)**

#### ENABLE/DISABLE

	INPUTS		0	UTPUTS
OEA	OEB	OEB	AO	B
L	X	Х	Hi Z	
Н	X	×	Active	
×	L	L		Inactive (H)
×	L	Н		Inactive (H)
×	Н	L		Active
×	Н	Н		Inactive (H)

#### **BUFFER**

INPUT	OUTPUT
L	Н
Н	L

#### LATCH

INPU	ОИТРИТ	
CLK/LE	DATA	COIPGI
Н	L	Н
н	Н	L
L	×	$Q_0$

#### LOOPBACK

LOOPBACK	qt
L	B port
н	Point P‡

<sup>†</sup>Q is the input to the B-to-A logic element.

#### SELECT

INPUTS		SELECTED LOGIC
MODE1	MODE0	ELEMENT
L	L	Buffer
L	Н	Flip-flop
Н	X	Latch

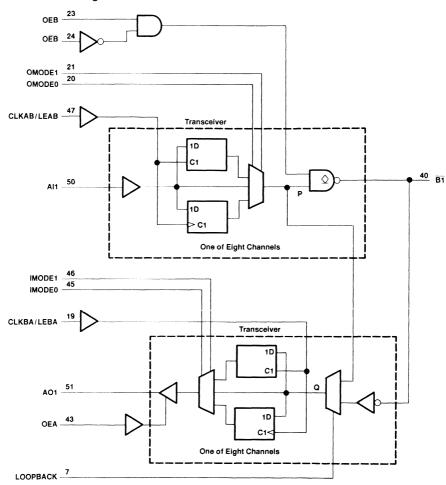
#### FLIP-FLOP

INPUTS		OUTPUT
CLK/LE	DATA	COTPOT
L	×	Q <sub>0</sub>
1	L	н
1	н	L



<sup>&</sup>lt;sup>‡</sup> P is the output of the A-to-B logic element (see functional block diagram).

## functional block diagram



Pin numbers shown are for the RC package.

## SN54FB2033, SN74FB2033A 8-BIT TTL/BTL REGISTERED TRANSCEIVERS

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> : except B port	1.2 V to 7 V
B port	1.2 V to 3.5 V
Input current range, (except B port)	
Voltage range applied to any B output in the disabled or power-off state	0.5 V to 3.5 V
Voltage range applied to any output in the high state: A port	0.5 V to V <sub>CC</sub>
Current applied to any single output in the low state: A port	48 mA
B port	200 mA
Maximum power dissipation at $T_A = 55$ °C (in still air) (see Note 1): RC package	1.4 W
Storage temperature range	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions (see Note 2)

			SN	54FB20	33	SN	74FB203	3A	LINUT	
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
V <sub>CC</sub> , BG V <sub>CC</sub>	Supply voltage		4.75	5	5.25	4.75	5	5.25	٧	
BIAS V <sub>CC</sub>	Supply voltage		4.5	5	5.5	4.5	5	5.5	V	
ViH	High Investigation of the con-	B̄ port	1.62*		2.3	1.62		2.3	V	
	High-level input voltage	Except B port	2		į.	2			· ·	
	law law line du plane	B̄ port	0.75	6	1.47*	0.75		1.47	v	
VIL	Low-level input voltage	Except B port		A <sup>3</sup>	0.8			0.8	ľ	
Юн	High-level output current	AO port		S.	-3			-3	mA	
1	Law level autout auront	AO port			24			24	mA	
OL	Low-level output current	B port	1 65		100			100	mA	
Δt/Δν	Input transition rise or fall rate	Except B port			10			10	ns/V	
T <sub>A</sub>	Operating free-air temperature		-55		125	0		70	°C	

<sup>\*</sup> On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not tested.



NOTE 1: The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 75 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

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#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	DADAMETED	TEST SOND	ITIONS	SN	154FB20	33	SN	74FB203	3A	UNIT	
	PARAMETER	TEST COND	IIIONS	MIN	TYPT	MAX	MIN	TYPT	MAX	UNII	
ViK		V <sub>CC</sub> = 4.75 V,	I <sub>I</sub> = -18 mA			-1.2			-1.2	٧	
		$V_{CC} = 4.75 \text{ V to } 5.25 \text{ V},$	lOH = -10 μA		V <sub>CC</sub> -1			V <sub>CC</sub> -1.1			
٧он	AO port	Von 475 V	I <sub>OH</sub> = -3 mA	2.5	2.85	3.4	2.5	2.85	3.4	V	
		V <sub>CC</sub> = 4.75 V	I <sub>OH</sub> = -32 mA	2			2				
	AO port	V <sub>CC</sub> = 4.75 V	IOL = 20 mA		0.33	0.5		0.33	0.5		
M	AO port	VCC = 4.75 V	IOL = 55 mA			0.8			8.0	v	
VOL		V 475 V	I <sub>OL</sub> = 100 mA	0.75		1.1	0.75		1.1	· ·	
	B port	V <sub>CC</sub> = 4.75 V	I <sub>OL</sub> = 4 mA	0.5			0.5				
lj.	Except B port	V <sub>CC</sub> = 0,	V <sub>I</sub> = 5.25 V	I		100			100	μА	
To a	Except B port	V <sub>CC</sub> = 5.25 V,	V <sub>I</sub> = 2.7 V			50			50	μА	
۱н	B port‡	V <sub>CC</sub> = 0 to 5.25 V,	V <sub>I</sub> = 2.1 V			100			100	00 00	
	Except B port	V <sub>CC</sub> = 5.25 V,	V <sub>I</sub> = 0.5 V	1	, i	-50			-50	μΑ	
HL	B̄ port‡	V <sub>CC</sub> = 5.25 V,	V <sub>I</sub> = 0.75 V			-100			-100	μΑ	
ЮН	B port	V <sub>CC</sub> = 0 to 5.25 V,	V <sub>O</sub> = 2.1 V			100			100	μА	
lozh	AO port	V <sub>CC</sub> = 5.25 V,	V <sub>O</sub> = 2.7 V			50			50	μА	
lozu	AO port	V <sub>CC</sub> = 5.25 V,	V <sub>O</sub> = 0.5 V			-50			-50	μА	
IOS§	AO port	V <sub>CC</sub> = 5.25 V,	V <sub>O</sub> = 0	- 40	-80	-150	- 40	-80	-150	mA	
Icc	All outputs on	V <sub>CC</sub> = 5.25 V,	IO = 0		45	90		45	70	mA	
Ci	Al port and control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND			5			5		pF	
Co	AO port	VO = VCC or GND		1	5			5		pF	
~ (	D	V <sub>CC</sub> = 0 to 4.75 V		1		8			6		
Cio	B port per P1194.0	V <sub>CC</sub> = 4.75 V to 5.25 V		1		8			6	pF	

#### live-insertion characteristics over recommended operating free-air temperature range (see Note 3)

DAD	AMETER		TEST CONDITIONS	SN54FB2033		SN74FB			
PAH	AMETER		TEST CONDITIONS	MIN	MAX	MIN	MAX	UNIT	
		V <sub>CC</sub> = 0 to 4.5 V	V <sub>B</sub> = 0 to 2 V, V <sub>I</sub> (BIAS V <sub>CC</sub> ) = 4.5 V to 5.5 V		400		400	_	
		V <sub>CC</sub> = 4.5 V to 5.5 V	VB = 0 to 2 V, VI (BIAS VCC) = 4.5 V to 5.5 V		. 10		10	μА	
v <sub>O</sub>	B port	V <sub>CC</sub> = 0,	V <sub>I</sub> (BIAS V <sub>CC</sub> ) = 4.5 V to 5.5 V	1.62	2.1	1.62	2.1	V	
		V <sub>CC</sub> = 0,	$V_{B} = 1 \text{ V}, \qquad V_{I} \text{ (BIAS V}_{CC}) = 4.5 \text{ V to } 5.5 \text{ V}$	-30		-1			
IO B port		V <sub>CC</sub> = 0 to 5.5 V,	OEB = 0 to 0.8 V		170		100	μΑ	
		V <sub>CC</sub> = 0 to 2.2 V,	OEB = 0 to 5 V		100		100		

NOTE 3: Power-up sequence is as follows: GND, BIASVCC, VCC.



<sup>†</sup> All typical values are at  $V_{CC}$  = 5 V. ‡ For I/O ports, the parameters  $I_{IH}$  and  $I_{IL}$  include the off-state output current.

<sup>§</sup> Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

Parameter is based on characterization data but is not tested.

## SN54FB2033, SN74FB2033A 8-BIT TTL/BTL REGISTERED TRANSCEIVERS

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)

		1	SN54F	B2033						
		V <sub>CC</sub> :		MIN	MAX	V <sub>CC</sub> =		MIN	MAX	UNIT
		MIN	MAX		ĺ	MIN	MAX			
fclock	Clock frequency	0	150	0	150	0	150	0	150	MHz
tw	Pulse duration, CLKAB/LEAB or CLKBA/LEBA	3.9		4.3		3.3		3.3		ns
t <sub>su</sub>	Setup time, data before CLKAB/LEAB or CLKBA/LEBA1	2.9		3.3		2.7		2.7		ns
t <sub>h</sub>	Hold time, data after CLKAB/LEAB or CLKBA/LEBA↑	1	100	1.3		0.7		0.7		ns

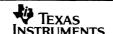
## SN54FB2033, SN74FB2033A 8-BIT TTL/BTL REGISTERED TRANSCEIVERS

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# switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)

	1			SN	54FB20	33			SN	74FB203	3A		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V(	CC = 5 V	!, ;	MIN	MAX	V <sub>0</sub>	CC = 5 V 4 = 25°C	!, :	MIN	MAX	UNIT
			MIN	TYP	MAX			MIN	TYP	MAX			
fmax			150			150		150			150		MHz
<sup>t</sup> PLH	Al	B	1.7	3.8	4.6	1.2	7.5	2.3	3.6	4.6	2.3	5.6	ns
<sup>t</sup> PHL	(thru mode)	В	1.3	2.6	4.3	1	5.5	1.9	3	4.2	1.9	4.5	113
<sup>†</sup> PLH	B	AO	2.5	3.9	5.9	1.4	7.6	2.5	4.2	5.5	2.5	6.1	ns
<sup>†</sup> PHL	(thru mode)	70	2.7	5.2	5.7	1.6	7.8	3	4.2	5.6	3	5.7	113
<sup>†</sup> PLH	Al	B	1.7	5	4.6	1.2	8.7	2.3	3.6	4.6	2.3	5.6	ns
<sup>†</sup> PHL	(transparent)	В	1.3	3.6	4.3	1	5.9	1.9	3	4.1	1.9	4.5	
tPLH	B	AO	2.5	4.3	5.8	1.5	7.8	2.5	4.2	5.5	2.5	6.1	nc
<sup>†</sup> PHL	(transparent)	AO	2.7	5.6	5.7	1.6	8	3	4.2	5.6	3	5.7	ns
<sup>†</sup> PLH	OEB	Ē	1.6	3.7	4.7	1.1	6.6	2.4	3.7	4.7	2.4	5.8	ns
<sup>†</sup> PHL	OEB	В	1.2	2.6	4.1	0.4	5.4	1.8	3	4.1	1.8	4.4	115
<sup>†</sup> PLH	OFF	Ē	1.3	3.8	4.3	1.2	6.6	2	3.4	4.3	2	5.2	ns
<sup>t</sup> PHL	OEB	В	1.2	2.9	4.4	0.8	5.5	2	3.3	4.4	2	4.8	115
<sup>t</sup> PZH	OEA	AO	2	3.5	5.1	1.2	6.6	2	3.5	4.6	2	5.1	
tPZL	OEA	AU	2.7	4.3	6.1	1.3	7.7	2.7	4.2	5.1	2.7	5.4	ns
t <sub>PHZ</sub>	054		2.1	3.5	5.8	1.1	6.9	2.1	4	5	2.1	5.5	
t <sub>PLZ</sub>	OEA	AO	1.6	2.7	4.7	1	6	1.6	2.8	3.9	1.6	4.3	ns
t <sub>PLH</sub>	011/4011540	-	2.1	5	5.8	1.6	8.7	3	4.7	5.8	3	6.9	
†PHL	CLKAB/LEAB	В	2	3.6	5.6	1.1	6.6	2.8	4.3	5.6	2.8	6.1	ns
tPLH	0		2	3.8	5.4	1.4	6.7	2	3.6	4.9	2	5.4	iii ns
†PHL	CLKBA/LEBA	AO	2.2	4.1	5.6	1.5	6.5	2.2	3.5	4.7	2.2	5.1	
<sup>†</sup> PLH	011005		2.3	4.8	6.1	1.6	8.1	2.4	5	6.1	2.4	7.2	
<sup>†</sup> PHL	OMODE	B	1.4	3.5	6	1	6.5	2.4	4.5	6	2.4	6.7	ns
tPLH	111005		1.8	3.6	5.9	1.3	7.3	1.8	4	5.3	1.8	5.9	
tPHL	IMODE	AO	2.3	4.1	5.4	1.4	6.4	2.3	4.1	5.2	2.3	5.4	ns
tPLH	LOOPPACK	40	2.4	4.6	7.1	1.6	8.3	2.4	5	7	2.4	8	
tPHL	LOOPBACK	AO	3.1	4.8	6.9	1.8	7.5	3.1	4.6	5.7	3.1	5.9	ns
<sup>t</sup> PLH		••	1.9	3.7	5.7	1.4	7.1	1.9	3.7	5.5	1.9	6.1	
<sup>t</sup> PHL	Al	AO	2.6	4.3	5.8	1.6	7.3	2.6	4.2	5.6	2.6	5.8	ns
	Rise time, 1.3 V to 1.8 V	B	0.5	1.5	2.1	0.4	3.2	0.5	1.2	2.1	0.5	3	
t <sub>t</sub>	Fall time, 1.8 V to 1.3 V	В	0.4	1.5	2.3	0.4	3.4	0.5	1.4	2.3	0.5	3	ns
ч	Rise time, 10% to 90%	AO	2	3.5	4.2	1.8	5.4	2	3.3	4.2	2	5	113
	Fall time, 90% to 10%		1	2.5	3.4	0.8	5.1	1	2.5	3.4	1	5	
tPR	B-port input pu	lse rejection				1.					1		ns

<sup>\*</sup> On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not tested.



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#### output-voltage characteristics

	DADAMETER	TEST	SN54FE	32033	SN74FB2033A		UNIT	
	PARAMETER	CONDITIONS	MIN	MAX	MIN	MAX	UNII	
V <sub>OHP</sub> †	Peak output voltage during turnoff of 100 mA into 40 nH				4		4.5	V
V <sub>OHV</sub> †	Minimum output voltage during turnoff of 100 mA into 40 nH	B port	See Figure 1	1.62		1.62		V
VOLV	Minimum output voltage during high-to-low switch	7	IOL = -50 mA	0.3		0.3		V

<sup>†</sup> Parameter is based on characterization data but not tested.

## PARAMETER MEASUREMENT INFORMATION

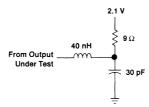
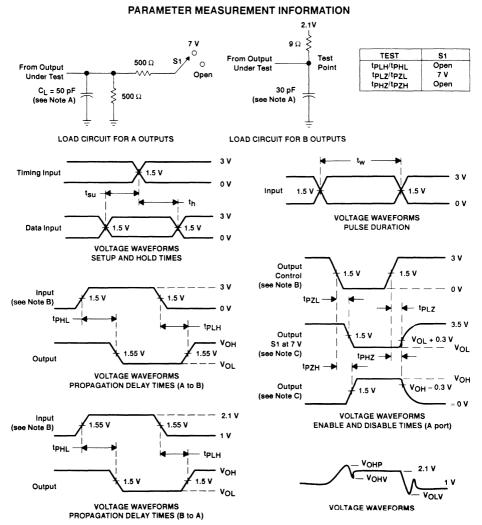


Figure 1. Load Circuit for VOHP, VOHV

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- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.
  - B. All input pulses are supplied by generators having the following characteristics: TTL inputs PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_f \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ , BTL inputs PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_f \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
  - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - D. The outputs are measured one at a time with one transition per measurement.

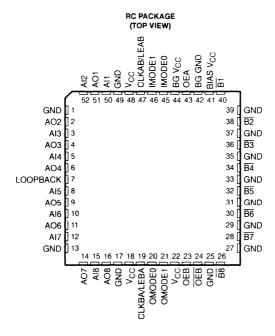
Figure 2. Load Circuits and Voltage Waveforms





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- TTL A Port, Backplane Transceiver Logic (BTL) B Port
- Open-Collector B-Port Outputs Sink 100 mA
- Isolated Logic-Ground and Bus-Ground Pins Reduce Noise
- BIAS V<sub>CC</sub> Pin Minimizes Signal Distortion During Live Insertion/Withdrawal
- B-Port Biasing Network Preconditions the Connector and PC Trace to the Backplane Transceiver Logic High-Level Voltage
- TTL-Input Structures Incorporate Active Clamping Networks to Aid in Line Termination
- Available in Plastic Quad Flatpack (RC) Package



#### description

The SN74FB2033H is an 8-bit transceiver featuring a split input (AI) and output (AO) bus on the TTL-level A port. The common I/O, open-collector  $\overline{B}$  port operates at backplane transceiver logic (BTL) signal levels.

The logic element for data flow in each direction is configured by two mode inputs (IMODE1 and IMODE0 for B-to-A, OMODE1 and OMODE0 for A-to-B) as a buffer, a D-type flip-flop, or a D-type latch. When configured in the buffer mode, the inverted input data appears at the output port. In the flip-flop mode, data is stored on the rising edge of the appropriate clock input (CLKAB/LEAB or CLKBA/LEBA). In the latch mode, the clock pins serve as active-high transparent latch enables.

Data flow in the B-to-A direction, regardless of the logic element selected, is further controlled by the LOOPBACK input. When LOOPBACK is low,  $\overline{B}$ -port data is the B-to-A input. When LOOPBACK is high, the output of the selected A-to-B logic element (prior to inversion) is the B-to-A input.



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## description (continued)

The AO port-enable/-disable control is provided by OEA. When OEA is low or when V<sub>CC</sub> is less than 2.5 V, the AO port is in the high-impedance state. When OEA is high, the AO port is active (high or low logic levels).

The  $\overline{B}$  port is controlled by OEB and  $\overline{OEB}$ . If OEB is low, or  $\overline{OEB}$  is high, or when  $V_{CC}$  is less than 2.5 V, the  $\overline{B}$  port is inactive. If OEB is high and  $\overline{OEB}$  is low, the B port is active.

BG V<sub>CC</sub> and BG GND are the bias-generator reference inputs.

The A-to-B and B-to-A logic elements are active regardless of the state of their associated outputs. The logic elements can enter new data (in flip-flop and latch modes) or retain previously stored data while the associated outputs are in the high-impedance (AO port) or inactive ( $\overline{B}$  port) states.

Output clamps are provided on the BTL outputs to reduce switching noise. One clamp reduces inductive ringing effects on  $V_{OH}$  during a low-to-high transition. The other clamps out ringing below the BTL  $V_{OL}$  voltage of 0.75 V. Both these clamps are active only during AC switching and do not affect the BTL outputs during steady-state conditions.

BIAS  $V_{CC}$  establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when  $V_{CC}$  is not connected. The SN74FB2033H is characterized for operation from 0°C to 70°C.

#### FUNCTION TABLE

					FUNCTION	IADLE			
				INPUTS				FUNCTION/MODE	
OEA	OEB	OEB	OMODE1	OMODE0	IMODE1	IMODE0	LOOPBACK	FUNCTION/MODE	
L	L	Х	Х	Х	Х	Х	Х	Isolation	
L	Χ	Н	Χ	X	Χ	X	×	isolation	
Х	Н	L	L	L	Х	Х	Х	Al to B, buffer mode	
Х	Н	L	L	Н	X	Х	X	Al to B, flip-flop mode	
Х	Н	L	Н	Х	Х	Х	×	Al to B, latch mode	
Н	L	Х	Х	Х	L	L	L	Ē. 10 b.#d	
Н	X	Н	X	X	L	L	L	B to AO, buffer mode	
Н	L	Х	Х	Х	L	Н	L	D to AO 455 floor mond	
Н	X	Н	Х	X	L	н	L	B to AO, flip-flop mode	
Н	L	X	X	Х	Н	X	L	B to AO, latch mode	
Н	Х	Н	Х	Х	Н	X	L	B to AO, latch mode	
Н	L	Х	Х	Х	L	L	H	Al to AO, buffer mode	
Н	Χ	Н	Х	Х	L	L	н	Ai to AO, buller mode	
Н	L	X	Х	X	L	Н	н	Al to AO, flip-flop mode	
Н	Х	Н	X	X	L	н	н	Ai to AO, ilip-liop mode	
Н	L	Х	Х	Х	Н	Х	н	Al to AO, latch mode	
Н	Χ	Н	X	X	Н	X	н	Ar to AO, laten mode	
Н	Н	L	Х	Х	X	X	L	Al to B, B to AO	



#### **Function Tables**

#### ENABLE/DISABLE

	INPUTS		OL	ITPUTS
OEA	OEB	OEB	AO	B
L	Х	Х	Hi Z	
Н	X	X	Active	
×	L	L		Inactive (H)
×	L	Н		Inactive (H)
х	Н	L		Active
Х	Н	Н		Inactive (H)

#### BUFFER

INPUT	OUTPUT
L	Н
н	L

#### LATCH

INPU	INPUTS					
CLK/LE	DATA	OUTPUT				
Н	L	Н				
н	н	L				
L	X	Q <sub>0</sub>				

#### LOOPBACK

LOOPBACK	Q†
L	B̄ port
н	Point P‡

<sup>†</sup> Q is the input to the B-to-A logic element.

#### SELECT

ĺ	INP	UTS	SELECTED-LOGIC
	MODE1	MODE0	ELEMENT
	L	Ł	Buffer
	L	Н	Flip-flop
	н	X	Latch

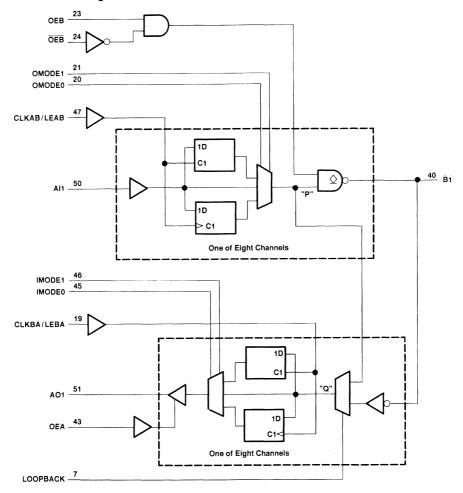
### FLIP-FLOP

INPU	TS	OUTDUT
CLK/LE	DATA	OUTPUT
L	Х	Q <sub>0</sub>
1	L	н
1	Н	L



<sup>‡</sup> P is the output of the A-to-B logic element (see functional block diagram).

## functional block diagram





## SN74FB2033H 8-BIT TTL/BTL REGISTERED TRANSCEIVER

SCBS472 - MAY 1994

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	$-0.5\ V$ to 7 $V$
Input voltage range, V <sub>I</sub> : except $\overline{B}$ port	
B port	1.2 V to 3.5 V
Input current range (except B port)	40 mA to 5 mA
Voltage range applied to any B output in the disabled or power-off state	0.5 V to 3.5 V
Voltage range applied to any output in the high state: A port	$\dots$ -0.5 V to V <sub>CC</sub>
Current applied to any single output in the low state: A port	48 mA
B̄ port	200 mA
Maximum power dissipation at $T_A = 55^{\circ}C$ (in still air)	1.4 W
Storage temperature range	65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### recommended operating conditions (see Note 1)

			MIN	NOM	MAX	UNIT
V <sub>CC</sub> , BG V <sub>CC</sub>	Supply voltage		4.75	5	5.25	V
BIAS V <sub>CC</sub>	Supply voltage		4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage		1.62		2.3	V
	riigh-level input voltage	Except B port	2			\ \ \
	Low-level input voltage	B̄ port	0.75		1.47	V
VIL	Low-level input voltage	Except B port			0.8	v
ЮН	High-level output current	AO port			-3	mA
1	Low lovel extent except	AO port			24	mA
IOL	Low-level output current	B port	1		100	IIIA
Δt/Δv	Input transition rise or fall rate	Except B port			10	ns/V
TA	Operating free-air temperature		0		70	°C

NOTE 1: Unused or floating pins (input or I/O) must be held high or low.



## SN74FB2033H 8-BIT TTL/BTL REGISTERED TRANSCEIVER

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### electrical characteristics over recommended operating free-air temperature range

	PARAMETER	TEST	CONDITIONS	MIN	TYPT	MAX	UNIT
VIK		V <sub>CC</sub> = 4.75 V,	í₁ = −18 mA			-1.2	V
		V <sub>CC</sub> = 4.75 V to 5.25 V,	IOH = −10 μA		1	/CC-1.1	
VOH	AO port	VCC = 4.75 V	IOH ≈ -3 mA	2.5	2.85	3.4	V
		VCC = 4.75 V	I <sub>OH</sub> ≈ -32 mA	2			
10	AO port	V <sub>CC</sub> = 4.75 V	I <sub>OL</sub> = 20 mA		0.33	0.5	
V	AC port	VCC = 4.75 V	I <sub>OL</sub> = 55 mA			0.8	V
VOL	5	V 4.75.V	I <sub>OL</sub> = 100 mA	0.75		1.1	ľ
B port		V <sub>CC</sub> = 4.75 V	IOL = 4 mA	0.5			
4	Except B port	V <sub>CC</sub> = 0,	V <sub>I</sub> = 5.25 V			100	μА
IH Except B port B port	V <sub>CC</sub> = 5.25 V,	V <sub>I</sub> = 2.7 V			50		
	B̄ port‡	V <sub>CC</sub> = 0 to 5.25 V,	V <sub>I</sub> = 2.1 V			100	μА
l	Except B port	V <sub>CC</sub> = 5.25 V,	V <sub>I</sub> = 0.5 V			-50	
ΊL	B port‡	V <sub>CC</sub> = 5.25 V,	V <sub>I</sub> = 0.75 V			-100	μА
ЮН	B port	V <sub>CC</sub> = 0 to 5.25 V,	V <sub>O</sub> = 2.1 V			100	μА
lozh	AO port	V <sub>CC</sub> = 5.25 V,	V <sub>O</sub> = 2.7 V			50	μА
lozL	AO port	V <sub>CC</sub> = 5.25 V,	V <sub>O</sub> = 0.5 V			-50	μА
IOS§	AO port	V <sub>CC</sub> = 5.25 V,	V <sub>O</sub> = 0	- 40	-80	-150	mA
lcc	All outputs on	V <sub>CC</sub> = 5.25 V,	IO = 0		45	70	mA
Ci	Al port and control inputs	V <sub>I</sub> ≈ V <sub>CC</sub> or GND			5		ρF
Co	AO port	VO = VCC or GND			5		pF
۰.	B port per P1194.0	V <sub>CC</sub> = 0 to 4.75 V				6	٥.
Cio <sup>¶</sup>	B poit per P1194.0	V <sub>CC</sub> = 4.75 V to 5.25 V				6	ρF

<sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ .

# timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)

		V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C	MIN	MAX	UNIT
		MIN MAX			ĺ
fclock	Clock frequency	0 150	0	150	MHz
t <sub>w</sub>	Pulse duration, CLKAB/LEAB or CLKBA/LEBA	3.3	3.3		ns
t <sub>su</sub>	Setup time, data before CLKAB/LEAB or CLKBA/LEBA↑	2.7	2.7		ns
th	Hold time, data after CLKAB/LEAB or CLKBA/LEBA↑	0.7	0.7		ns

For I/O ports, the parameters I<sub>IH</sub> and I<sub>IL</sub> include the off-state output current.

<sup>9</sup> Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

Parameter is based on characterization data but is not tested.

## SN74FB2033H 8-BIT TTL/BTL REGISTERED TRANSCEIVER

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)

PARAMETER	FROM	TO	V <sub>0</sub>	CC = 5 \ A = 25°C	<i>'</i> ,	MIN	MAX	UNIT
	(INPUT)	(OUTPUT)	MIN	TYP	MAX			
f <sub>max</sub>			150			150		MHz
<sup>t</sup> PLH	ALG:	=	2.8	5.1	6.8	2.8	8.1	
tPHL .	Al (thru mode)	B	2.5	4.2	5.7	2.5	6.1	ns
<sup>t</sup> PLH	5.41	AO	2.2	4.3	6	2.2	6.6	
<sup>†</sup> PHL	B (thru mode)	AO	2.6	4.2	5.6	2.6	6	ns
<sup>t</sup> PLH	Al (transparent)		2.8	5.1	6.8	2.8	8.1	
tPHL	Al (transparent)	B	2.6	4.2	5.7	2.6	6.1	ns
<sup>†</sup> PLH	8		2.2	4.3	6	2.2	6.6	
tPHL	B (transparent)	AO	2.5	4.2	5.6	2.5	6	ns
tPLH .	050	-	2.7	5.1	6.8	2.7	8.3	
tPHL	OEB	B	2.4	4.2	5.7	2.4	6.1	ns
†PLH	2	_	2.5	4.8	6.4	2.5	7.7	
tPHL	ÖEB	B	2.5	4.3	5.9	2.5	6.4	ns
<sup>t</sup> PZH	054	OEA AO	1.6	3.6	5.1	1.6	5.6	ns
tPZL	OEA		2.3	4.3	5.7	2.3	6	
<sup>t</sup> PHZ	054		1.7	4	5.5	1,7	5.9	
tPLZ	OEA	AO	1.2	2.9	4.4	1.2	4.7	ns
<sup>t</sup> PLH	OLKARII SAR	=	3.7	6.5	8.3	3.7	9.9	
tPHL	CLKAB/LEAB	B	3.4	5.4	7.1	3.4	7.7	ns
tPLH	CLVDA# EDA	40	4.7	3.8	5.5	4.7	5.9	
<sup>†</sup> PHL	CLKBA/LEBA	AO	4.8	3.6	5.1	4.8	5.5	ns
<sup>t</sup> PLH	OHORE	=	2.9	6.6	8.4	2.9	10	
tPHL	OMODE	B	3	5.7	7.5	3	8.3	ns
<sup>t</sup> PLH	11005		1.4	4.1	5.8	1.4	6.4	
tPHL	IMODE	AO	1.9	4.2	5.7	1.9	5.9	ns
tPLH	LOOPPACK	40	2	5.2	7.3	2	8.2	
<sup>†</sup> PHL	LOOPBACK	AO	2.6	4.8	6.3	2.6	6.4	ns
<sup>†</sup> PLH			1.7	3.9	5.6	1.7	6.1	
tPHL	Al	AO	2.2	4.3	5.7	2.2	5.9	ns
	Rise time, 1.3 V to 1.8 V	_	1.8	2.5	3.8	1.7	4	
	Fall time, 1.8 V to 1.3 V	B	1.7	2.5	3.8	1.5	4	
tţ	Rise time, 10% to 90%	4.0	2.5	3.4	4.8	2	5	ns
	Fall time, 90% to 10%	AO	1.5	2.5	3.8	1	5	
tpR	B-port input pulse rejection		1			1		ns



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# live-insertion characteristics over recommended operating free-air temperature range (see Note 2)

F	ARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
$V_{CC} = 0 \text{ to } 4.5 \text{ V}$ $V_{B} = 0 \text{ to } 2 \text{ V}$ $V_{B} = 0 \text{ to } 2 \text{ V}$ $V_{CC} = 4.5 \text{ V} \text{ to } 5.5 \text{ V}$ $V_{CC} = 4.5 \text{ V} \text{ to } 5.5 \text{ V}$		V <sub>CC</sub> = 0 to 4.5 V	'CC = 0 to 4.5 V V <sub>R</sub> = 0 to 2 V,		400	μА
		BIAS V <sub>CC</sub> = 4.5 V to 5.5 V		10	μΑ	
Vo	B port	V <sub>CC</sub> = 0,	BIAS V <sub>CC</sub> = 4.5 V to 5.5 V	1.62	2.1	V
		V <sub>CC</sub> = 0, V <sub>I</sub> (BIAS V <sub>CC</sub> ) = 4.5 V to 5.5 V	V <sub>B</sub> = 1 V,	-1		
IO B port	B port	V <sub>CC</sub> = 0 to 5.5 V,	OEB = 0 to 0.8 V		100	μА
	1	V <sub>CC</sub> = 0 to 2.2 V,	OEB = 0 to 5 V		100	

NOTE 2: Power-up sequence is as follows: GND, BIASVCC, VCC.

## switching characteristics (see Figure 2)

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT	
V <sub>OHP</sub> †	Peak output voltage during turnoff of 100 mA into 40 nH	B port	See Figure 1		3	V
V <sub>OHV</sub> †	Minimum output voltage during turnoff of 100 mA into 40 nH	B port	See Figure 1	1.62		٧
VOLV	Minimum output voltage during high-to-low switch	B port	I <sub>OL</sub> = -50 mA	0.3		V

<sup>†</sup> Parameter is based on characterization data but not tested.

#### PARAMETER MEASUREMENT INFORMATION

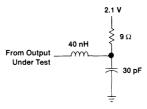
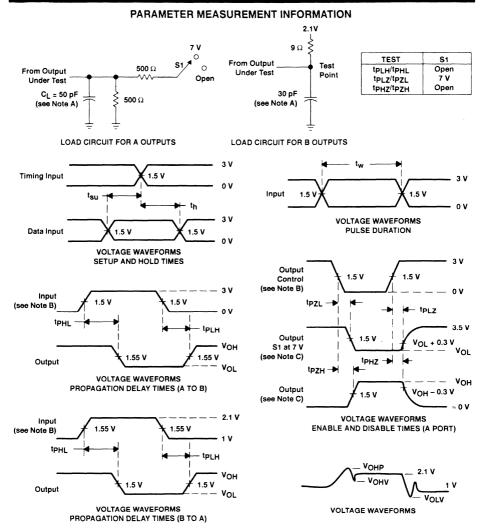


Figure 1. Load Circuit for VOHP, VOHV





- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.
  - B. All input pulses are supplied by generators having the following characteristics: TTL inputs PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>f</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns, BTL inputs PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>f</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
  - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - D. The outputs are measured one at a time with one transition per measurement.

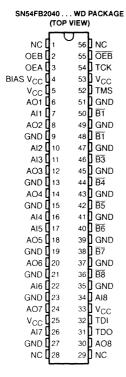
Figure 2. Load Circuit and Voltage Waveforms

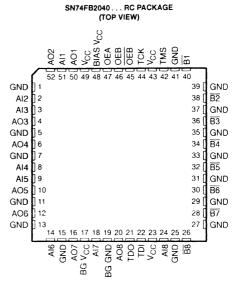




SCBS173B - NOVEMBER 1991 - REVISED SEPTEMBER 1994

- Compatible With IEEE 1194.1-1991 (BTL) Standard
- TTL A Port, Backplane Transceiver Logic
   R Port
- Open-Collector B-Port Outputs Sink 100 mA
- Isolated Logic-Ground and Bus-Ground Reduces Noise
- BIAS V<sub>CC</sub> Pin Minimizes Signal Distortion During Live Insertion/Withdrawal
- B-Port Biasing Network Preconditions the Connector and PC Trace to the Backplane Transceiver Logic High-Level Voltage
- Package Options Include Plastic Quad Flat (RC) Package and Ceramic Flat (WD) Package





NC - No internal connection

#### description

The 'FB2040 are 8-bit transceivers designed to translate signals between TTL and backplane transceiver logic (BTL) environments.

The  $\overline{B}$  port operates at BTL-signal levels. The open-collector  $\overline{B}$  ports are specified to sink 100 mA. Two output enables, OEB and  $\overline{OEB}$ , are provided for the  $\overline{B}$  outputs. When OEB is high and  $\overline{OEB}$  is low, the  $\overline{B}$  port is active and reflects the inverse of the data present at the A-input pins. When OEB is low,  $\overline{OEB}$  is high, or  $V_{CC}$  is typically less than 2.5 V, the  $\overline{B}$  port is turned off.



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#### description (continued)

The A port operates at TTL-signal levels and has split input and output pins. The A outputs reflect the inverse of the data at the  $\overline{B}$  port when the A-port output enable, OEA, is high. When OEA is low or when  $V_{CC}$  is typically less than 2.5 V, the A outputs are in the high-impedance state.

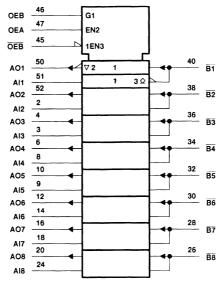
Pins are allocated for the four-wire IEEE 1149.1 (JTAG) test bus. Currently, TMS and TCK are not connected and TDI is shorted to TDO.

BIAS  $V_{CC}$  establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when  $V_{CC}$  is not connected.

The SN54FB2040 is characterized for operation over the full military temperature range of ~55°C to 125°C. The SN74FB2040 is characterized for operation from 0°C to 70°C.

		FUI	NCTION TABLE			
	INPUTS		FUNCTION			
OEB	OEB	OEA	FUNCTION			
L X	X H	L L	Isolation			
L	X H	Н	B data to AO bus			
Н	L	L	Al data to B bus			
Н		Н	Al data to B bus. B data to AO bus			

#### logic symbol†

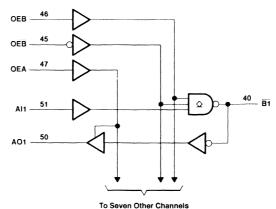


<sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the RC package



2-68

## functional block diagram



To Seven Other Ch

Pin numbers shown are for the RC package.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> : except B port	1.2 V to 7 V
B̄ port	1.2 V to 3.5 V
Input current range (except B port)	40 mA to 5 mA
Voltage range applied to any $\overline{B}$ output in the disabled or power-off state	$-0.5$ V to $5.5$ V
Voltage range applied to any output in the high state	$\dots$ -0.5 V to V <sub>CC</sub>
Current applied to any single output in the low state: A port	48 mA
B port	200 mA
Operating free-air temperature range, T <sub>A</sub> : SN54FB2040	55°C to 125°C
SN74FB2040	
Maximum power dissipation at $T_A = 55^{\circ}C$ (in still air) (see Note 1): RC package	1.4 W
Storage temperature range	. −65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.



NOTE 1: The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 75 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

## SN54FB2040, SN74FB2040 8-BIT TTL/BTL TRANSCEIVERS

SCBS173B - NOVEMBER 1991 - REVISED SEPTEMBER 1994

#### recommended operating conditions (see Note 2)

			SN	SN54FB2040 SN74FB2040			40	UNIT		
			MIN	NOM	M MAX MIN NOM MA		MAX	רוואט ר		
V <sub>CC</sub> , BIAS V <sub>CC</sub> , BG V <sub>CC</sub>	Supply voltage		4.75	5	5.25	4.5	5	5.5	V	
	Disk leading to the second	B port*	1.62		2.3	1.62		2.3	v	
VIH	High-level input voltage	Except B port	2			2				
		B port*	0.75		1.47	0.75		1.47	V	
VIL	Low-level input voltage	Except B port			0.8			0.8		
lik	Input clamp current				-18			-18	mA	
Юн	High-level output current	AO port						-3	mA	
		AO port						24	^	
IOL	Low-level output current	B port			100			100	mA	
TA	Operating free-air temperature		-55		125	0		70	°C	

<sup>\*</sup> On products compliant to MIL-STD-833, Class B, this parameter is based on characterization data but is not tested.

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

		TEST OF	TEST CONDITIONS		54FB20	40	SN	74FB20	40	UNIT	
	PARAMETER	TEST CO	DNDITIONS	MIN	TYPT	MAX	MIN	TYPT	MAX	UNII	
	B port	V 45V	I <sub>I</sub> = -18 mA			-1.2			-1.2	V	
VIK	Except B port	V <sub>CC</sub> = 4.5 V	I <sub>I</sub> = -40 mA			-1.2			-0.5	٧	
	AO port	V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = -1 mA		3.2					V	
VOH AO	AO port	VCC = 4.5 V	I <sub>OH</sub> = -3 mA	2.5	3.3		2.5	3.3			
	AO port	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 20 mA		0.09					\ <sub>v</sub>	
VOL	AO port	VCC = 4.5 V	I <sub>OL</sub> = 24 mA		0.35	0.5		0.35	0.5		
VOL	B̄ port	V <sub>CC</sub> = 4.5 V	IOL = 80 mA	0.75		1.1	0.75		1.1	,	
		VCC = 4.5 V	I <sub>OL</sub> = 100 mA			1.2			1.15		
l <sub>l</sub>	Except B port	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> ≈ 5.5 V			50			50	μА	
liH‡	Except B port	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 2.7 V			50			50	μА	
. +	Except B port		V <sub>I</sub> = 0.5 V			-50			-50		
I <sub>IL</sub> ‡	B port	V <sub>CC</sub> = 5.5 V	V <sub>I</sub> ≈ 0.75 V			-100			-100	μА	
ЮН	B̄ port	V <sub>CC</sub> = 0 to 5.5 V,	V <sub>O</sub> = 2.1 V			100			100	μА	
lozh	AO port	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V			50			50	μА	
lozL	AO port	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V			-50			-50	μА	
IOS§	AO port	V <sub>CC</sub> = 5.5 V,	VO = 0	- 30		-170	- 30		-180	mA	
la a	Al port to B port	V 55V	1- 0		25	40		40		mA	
Icc	B port to AO port	V <sub>CC</sub> = 5.5 V,	IO = 0		60	70		70		mA	
Ci	Al port*	VI = VCC or GND			25	70		3.5		pF	
5	Control inputs*	J AL = ACC OLGUAD				9.9		3		ρr	
Со	AO port*	VO = VCC or GND				14.7		6		рF	
Cia	B port per P1194.0*	V <sub>CC</sub> = 0 to 4.5 V				8			5	pF	
Cio	b port per P1194.0	V <sub>CC</sub> = 4.5 V to 5.5 V				9			5		

<sup>\*</sup> On products compliant to MIL-STD-833, Class B, this parameter is based on characterization data but is not tested.

<sup>§</sup> Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.



 $<sup>^{\</sup>dagger}$  All typical values are at VCC = 5 V, TA = 25°C.

For I/O ports, the parameters I<sub>IH</sub> and I<sub>IL</sub> include the off-state output current.

## SN54FB2040, SN74FB2040 8-BIT TTL/BTL TRANSCEIVERS

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## live-insertion specifications over recommended operating free-air temperature range

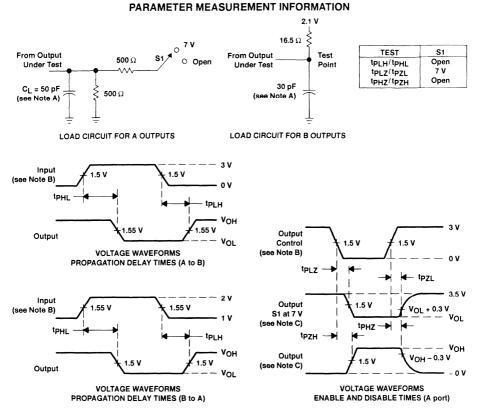
PARAMETER			TEST CONDITIONS			SN74FB2040		UNIT
			TEST CONDITIONS	MIN	MAX	MIN	MAX	CIVIT
1(0	146 //)	V <sub>CC</sub> = 0 to 4.5 V	V- 04-0V W (DIAC V-) A 5 V 4-5 5 V		450		450	
ICC (p	IAS V <sub>CC</sub> )	V <sub>CC</sub> = 4.5 to 5.5 V	$V_B = 0 \text{ to } 2 \text{ V}, V_I \text{ (BIAS V}_{CC}) = 4.5 \text{ V to } 5.5 \text{ V}$	10 10		μА		
ν <sub>O</sub>	B port	VCC = 0,	V <sub>I</sub> (BIAS V <sub>CC</sub> ) = 4.5 V to 5.5 V	1.62	2.1	1.62	2.1	V
		V <sub>CC</sub> = 0,	$V_B = 1 \text{ V}, \qquad V_I \text{ (BIAS V}_{CC}) = 4.5 \text{ V to } 5.5 \text{ V}$	-30		-1		
10	B port	$V_{CC} = 0 \text{ to } 5.5 \text{ V},$	OEB = 0 to 0.8 V	1	100		100	μА
	1	$V_{CC} = 0 \text{ to } 2.2 \text{ V},$	OEB = 0 to 5 V		100		100	

# switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		CC = 5 \ \ = 25°C		SN54FB2040		SN74FB2040		UNIT
	(1147-01)	(001701)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<sup>†</sup> PLH	Al	Ē	3.2	4.5	6	0.5	8.5	2.4	6.5	
<sup>t</sup> PHL	<b>1</b>	В	2.8	4.2	5.6	0.4	8.5	2.7	5.8	ns
<sup>t</sup> PLH	Ē	AO	2.3	3.8	5.7	0.4	8	1.9	6.2	
<sup>t</sup> PHL	В	AU.	2.3	4.2	5.9	0.8	14.9	2	8.2	ns
<sup>†</sup> PLH	OEB	Ĕ	3.7	5.1	6.7	0.5	9.9	3	7	ns
<sup>t</sup> PHL	OEB	В	3.1	4.6	5.9	0.4	9.5	3	6.1	ris.
<sup>†</sup> PLH	ŌĒB	B	3.6	5.2	6.8	1.3	9.5	3.3	7	ns
<sup>t</sup> PHL	OEB		2.9	4.4	5.9	0.2	9.8	2.6	6.1	
<sup>t</sup> PZH	OEA	AO	2.5	4	5.5	1.2	8	2.1	5.8	ns
<sup>t</sup> PZL	OLA	40	2.1	3.6	4.8	0.8	7.5	2	5	115
<sup>(</sup> PHZ	OEA	AO	2.3	4.1	5.9	1	8.2	1.9	6.5	
<sup>t</sup> PLZ	OLA	**	1.6	3.1	4.5	0.4	7.2	1.4	4.7	ns
t <sub>sk(p)</sub> •	Skew for any single channel	Al to $\overline{B}$ or $\overline{B}$ to AO		0.5						ns
<sup>t</sup> sk(o)*	Skew between drivers in the same package	Al to B or B to AO		0.4			2			ns
	Rise time, 1.3 V to 1.8 V	5	2	2.8	3.8	0.2	4.5	1.7		
tţ	Fall time, 1.8 V to 1.3 V	B	1	1.9	3	0.9	4.0	1	4.2	
tPR.	B-port input pulse rejection							1	3.4	ns

<sup>\*</sup> On products compliant to MIL-STD-833, Class B, this parameter is based on characterization data but is not tested.





- NOTES: A. C<sub>I</sub> includes probe and jig capacitance.
  - B. All input pulses are supplied by generators having the following characteristics: TTL inputs PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_f \leq$  2.5 ns,  $t_f \leq$  2.5 ns. BTL inputs PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_f \leq$  2.5 ns,  $t_f \leq$  2.5 ns.
  - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - D. The outputs are measured one at a time with one transition per measurement.

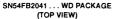
Figure 1. Load Circuits and Voltage Waveforms

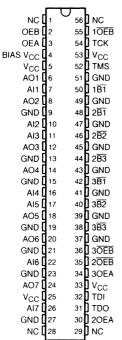


SCBS172B - NOVEMBER 1991 - REVISED SEPTEMBER 1994

- Compatible With IEEE 1194.1-1991 (BTL) Standard
- TTL A Port, Backplane Transceiver Logic
- Open-Collector B-Port Outputs Sink 100 mA
- Isolated Logic-Ground and Bus-Ground Reduces Noise
- BIAS V<sub>CC</sub> Pin Minimizes Signal Distortion During Live Insertion/Withdrawal
- B-Port Biasing Network Preconditions the Connector and PC Trace to the Backplane Transceiver Logic High-Level Voltage
- Package Options Include Plastic Quad Flat (RC) Package and Ceramic Flat (WD) Package

SN74FB2041 . . . RC PACKAGE





(TOP VIEW) 10EA 52 51 50 49 48 47 46 45 44 43 42 41 40 GND **GND** 39 [ 2AI1 2 38 2B1 **GND** 2AI2 3 37 2AO2 2B2 36 GND 35 GND 2AO3 34 2B3 **GND** 33 f GND 2AI3 8 32 3B1 3AI1 19 31 GND 3AO1 10 30 [ 3B2 GND 29 [ GND 3AO2 12 28  $3\overline{B3}$ GND 13 **GND** 14 15 16 17 18 19 20 21 22 23 24 25 26 3AI3 GND 20EA 3A03 200

NC - No internal connection

#### description

The 'FB2041 are 7-bit transceivers designed to translate signals between TTL and backplane transceiver logic (BTL) environments.

The  $\overline{B}$  port operates at BTL-signal levels. The open-collector  $\overline{B}$  ports are specified to sink 100 mA. Two output enables, OEB and  $\overline{OEB}$ , are provided for the  $\overline{B}$  outputs. When OEB is high and  $\overline{OEB}$  is low, the  $\overline{B}$  port is active and reflects the inverse of the data present at the A-input pins. When OEB is low,  $\overline{OEB}$  is high, or  $V_{CC}$  is typically less than 2.5 V, the  $\overline{B}$  port is turned off. The enable/disable logic partitions the device as two 3-bit sections and one 1-bit section.



## SN54FB2041, SN74FB2041 7-BIT TTL/BTL TRANSCEIVERS

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#### description (continued)

The A port operates at TTL-signal levels and has split input and output pins. The A outputs reflect the inverse of the data at the  $\overline{B}$  port when the A-port output enable, OEA, is high. When OEA is low or when  $V_{CC}$  is typically less than 2.5 V, the A outputs are in the high-impedance state.

Pins are allocated for the four-wire IEEE 1149.1 (JTAG) test bus. Currently, TMS and TCK are not connected and TDI is shorted to TDO.

BIAS V<sub>CC</sub> establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when V<sub>CC</sub> is not connected.

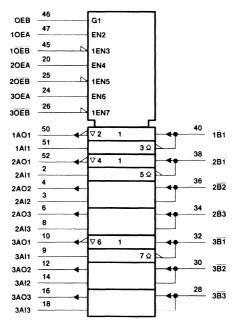
The SN54FB2041 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74FB2041 is characterized for operation from 0°C to 70°C.

#### **FUNCTION TABLE**

	101011011111111										
	INPUTS		FUNCTION								
OEB	OEB	OEA	FONCTION								
L	X H	L L	Isolation								
L X	X H	H	B data to AO bus								
Н	Ł	L	Al data to B bus								
Н	L	Н	$\overline{AI}$ data to B bus, $\overline{B}$ data to AO bus								



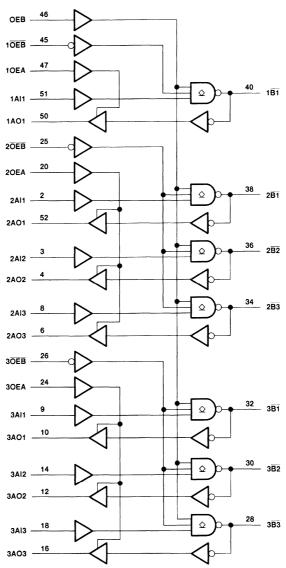
## logic symbol†



<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the RC package.



## functional block diagram



Pin numbers shown are for the RC package.



2-76

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ 0.5 V to 7 V Input voltage range, $V_{I}$ : except $\overline{B}$ port1.2 V to 7 V	
B port –1.2 V to 3.5 V	/
Input current range (except B port) ————————————————————————————————————	
Voltage range applied to any B output in the disabled or power-off state0.5 V to 5.5 V	/
Voltage range applied to any output in the high state	7
Current applied to any single output in the low state: A port	ĺ
É port	١
Operating free-air temperature range, T <sub>A</sub> : SN54FB2041	)
SN74FB2041 0°C to 70°C	2
Maximum power dissipation at $T_A = 55^{\circ}$ C (in still air) (see Note 1): RC package	V
Storage temperature range ——65°C to 150°C	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions (see Note 2)

			SN54FB2041			SN74FB2041			LINUT	
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
V <sub>CC</sub> , BIAS V <sub>CC</sub> , BG V <sub>CC</sub>	Supply voltage		4.5	5	5.5	4.5	5	5.5	٧	
	High level in the land	B port	1.62		2.3	1.62		2.3	٧	
VIH	High-level input voltage	Except B port	2		7	2				
V	Low lovel input veltage	B port	0.75	- 42	1.47	0.75		1.47	.,,	
VIL	Low-level input voltage	Except B port		- 6	0.8			8.0	V	
lik	Input clamp current				~18			-18	mA	
ЮН	High-level output current	AO port		ý.	-3		***************************************	-3	mA	
1	Low lovel autout average	AO port			24			24		
OL	Low-level output current	B port			100			100	mA	
TA	Operating free-air temperature		-55		125	0		70	°C	

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

NOTE 1: The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 75 mils. For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SGBD002B.

## SN54FB2041, SN74FB2041 7-BIT TTL/BTL TRANSCEIVERS

SCBS172B - NOVEMBER 1991 - REVISED SEPTEMBER 1994

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	DARAMETER	TEST OF	TEST CONDITIONS		54FB20	41	SN	74FB20	41	UNIT	
ĺ	PARAMETER	1EST CO	SNOTTIONS	MIN	TYPT	MAX	MIN	TYPT	MAX	UNIT	
.,	B port	V 45V	I <sub>I</sub> = -18 mA			-1.2			-1.2	V	
VIK	Except B port	V <sub>CC</sub> = 4.5 V	I <sub>I</sub> = -40 mA			-0.5			-0.5	V	
1/	AO port	V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = -1 mA							V	
VOH	AC port	VCC = 4.5 V	I <sub>OH</sub> = -3 mA	2.5	3.3		2.5	3.3		ı v	
	AO port	V <sub>CC</sub> = 4.5 V	IOL = 20 mA							v	
\/ -	AO pon	V()() = 4.5 V	I <sub>OL</sub> = 24 mA		0.35	0.5		0.35	0.5		
VOL	~ .	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 80 mA	0.75		1.1	0.75		1.1	٧	
	B port	VCC = 4.5 V	I <sub>OL</sub> = 100 mA			1.15			1.15		
l <sub>l</sub>	Except B port	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 5.5 V			50			50	μА	
\lH <sup>‡</sup>	Except B port	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 2.7 V		48	50			50	μА	
. +	Except B port		V <sub>I</sub> = 0.5 V		3	-50			-50		
l <sub>IL</sub> ‡	B port	V <sub>CC</sub> = 5.5 V	V <sub>I</sub> = 0.75 V		\$7	-100			-100	μА	
ЮН	B port	V <sub>CC</sub> = 0 to 5.5 V,	V <sub>O</sub> = 2.1 V	- A	7	100			100	μА	
lozh	AO port	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V			50			50	μΑ	
lozu	AO port	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V			-50			-50	μА	
los§	AO port	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0	-30		-150	- 30		-180	mA	
	Al port to B port	V . 55V			25			40		mA	
ICC	B port to AO port	V <sub>CC</sub> = 5.5 V,	1O = 0		65			65		mA	
C.	Al port	Vi. Vacar CND						3.5		pF	
Ci	Control inputs	VI = VCC or GND						3		ρr	
Со	AO port	VO = VCC or GND						6		pF	
C	B port per P1194.0	V <sub>CC</sub> = 0 to 4.5 V				6			5	pF	
Cio	B port per P1194.0	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$				5			5	pr	

## live-insertion specifications over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS			SN54FB2041		SN74FB2041		
		1531	CONDITIONS	MIN	MAX	MIN	MAX	UNIT	
ICC (BIAS VCC)		V <sub>CC</sub> = 0 to 4.5 V	V <sub>B</sub> = 0 to 2 V,	450		450			
ICC (B)	W2 ACC)	V <sub>CC</sub> = 4.5 V to 5.5 V	$V_{I}$ (BIAS $V_{CC}$ ) = 4.5 V to 5.5 V	<u>ે</u> 10		10		μА	
VO	B̄ port	V <sub>CC</sub> = 0,	V <sub>I</sub> (BIAS V <sub>CC</sub> ) = 4.5 V to 5.5 V	1.62	2.1	1.62	2.1	٧	
la.		V <sub>CC</sub> = 0, V <sub>B</sub> = 1 V, V <sub>I</sub> (BIAS V <sub>CC</sub> ) = 4.5 V to 5.5 V		-1		-1			
10	B port	V <sub>CC</sub> = 0 to 5.5 V,	OEB = 0 to 0.8 V		100		100	μА	
		V <sub>CC</sub> = 0 to 2.2 V,	OEB = 0 to 5 V	(C)	100		100		



<sup>†</sup> All typical values are at V $_{CC}$  = 5 V, T $_{A}$  = 25°C. ‡ For I/O ports, the parameters I $_{IH}$  and I $_{IL}$  include the off-state output current.

<sup>§</sup> Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

## SN54FB2041, SN74FB2041 7-BIT TTL/BTL TRANSCEIVERS

SCBS172B - NOVEMBER 1991 - REVISED SEPTEMBER 1994

# switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		CC = 5 V 4 = 25°C		SN54FB2041		SN74FB2041		UNIT
	(1147-01)	(001701)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	1
<sup>†</sup> PLH	Al	-	3	4.6	6			2.7	6.5	ns
t <sub>PHL</sub>	1 ^'	B	2.7	4.2	5.6			2.5	5.8	ns
tPLH		AO	2.2	3.7	5.5			1.8	6	ns
t <sub>PHL</sub>	В	AU	2.6	4.1	5.9			2.2	7.9	115
<sup>†</sup> PLH	OEB	5	3.8	5.3	7.1			3.3	7.4	
t <sub>PHL</sub>		В	3.4	4.9	6.5			3.2	6.7	ns
†PLH	OEB	B	3.7	5.1	6.8			3.4	7	ns
<sup>†</sup> PHL		В	2.9	4.4	6.2			2.4	6.4	
<sup>t</sup> PZH	OEA	AO	1.8	3.3	5.1			1.5	5.6	ns
†PZL	]		1.7	3.1	4.7	- 3		1.6	5	
†PHZ	OEA	AO	1.9	3.3	5	100		1.3	5.3	ns
<sup>t</sup> PLZ	1 064	AO	1.1	2.6	4.3			0.9	4.7	
<sup>t</sup> sk(p)	Skew for any single channel   tpHL - tpLH	Al to B or B to AO		0.5						ns
<sup>t</sup> sk(o)	Skew between drivers in the same package	Al to $\overline{B}$ or $\overline{B}$ to AO		0.4						ns
	Rise time, 1.3 V to 1.8 V	5	2.4	3.5	4.6			2.2	5.2	
tt	Fall time, 1.8 V to 1.3 V	B	1	2	3			1	3.4	
tPR	B-port input pulse rejection	1				1		1		ns



#### PARAMETER MEASUREMENT INFORMATION 2.1 V **16.5** Ω TEST S1 From Output From Output Test 500 Ω tPLH/tPHL Open **Under Test Under Test** Point 7 V tPLZ/tPZL tPHZ/tPZH Open 30 pF C<sub>L</sub> = 50 pF 500 $\Omega$ (see Note A) (see Note A) LOAD CIRCUIT FOR A OUTPUTS LOAD CIRCUIT FOR B OUTPUTS Input 1.5 V 1.5 V (see Note B) οv Vон 3 V 1.55 V .55 V Output Output VOL Control **VOLTAGE WAVEFORMS** (see Note B) PROPAGATION DELAY TIMES (A to B) tp7i 3 5 V input Output 1.55 V 1.55 V VOL + 0.3 V (see Note B) S1 at 7 V VOL (see Note C) tpHZ <sup>t</sup>PZH Vон Vон Output ~ 0.3 V 15 V (see Note C) Output VOL - 0 V **VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS** PROPAGATION DELAY TIMES (B to A) **ENABLE AND DISABLE TIMES (A port)**

NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: TTL inputs PRR  $\leq$  10 MHz,  $Z_O \approx 50 \Omega$ ,  $t_f \leq 2.5$  ns. BTL inputs PRR  $\leq$  10 MHz,  $Z_O \approx 50 \Omega$ ,  $t_f \leq 2.5$  ns.  $t_f \leq 2.5$  ns.  $t_f \leq 2.5$  ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms



ETL Enhanced Transceiver Logic	1
BTL Backplane Transceiver Logic	2
GTL Gunning Transceiver Logic	3
ABT/CBT 25- $\Omega$ Incident-Wave Switching Drivers	4
Mechanical Data	5

The new TI Gunning Transceiver Logic (GTL) family allows designers of high-performance workstation and networking equipment to achieve higher speeds with much less power-consumption overhead. GTL transceivers use a 0.8 V output switching region with a very small (100 mV) input threshold, to handle device speeds as high as 150 MHz. Applications are GTL backplanes that require TTL translation, memory array point-to-point drivers, and local-bus interface drivers between a GTL processing system and a TTL bus.

## SN54GTL16612, SN74GTL16612 18-BIT GTL/LVT UNIVERSAL BUS TRANSCEIVERS

SCBS480B - JUNE 1994 - REVISED OCTOBER 1994

•	Translates Between GTL Logic Levels and
	LVTTL or 5-V TTL Logic Levels

- Members of the Texas Instruments Widebus™ Family
- Support Mixed-Mode Signal Operation on A Port
- Universal Bus Transceiver (UBT™)
   Combines D-Type Latches and D-Type
   Flip-Flops With Qualified Storage Enable
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors on A Port
- Flow-Through Architecture Optimizes
   Printed-Circuit-Board Layout
- Package Options Include Plastic Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Ceramic Flat (WD) Packages

#### description

These 18-bit bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

The B port operates at GTL levels while the A port and control pins are compatible with LVTTL or 5-V TTL logic levels.

Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock or latch-enable can be controlled by the clock-enable (CEAB and CEBA) inputs. For A-to-B data flow, the devices operate

#### SN54GTL16612... WD PACKAGE SN74GTL16612... DGG OR DL PACKAGE (TOP VIEW)

OEAB [	I₁ ∪	56	CEAB
LEAB [		55	CLKAB
A1 [	3	54	B1
GND [	4	53	] GND
A2 [		52	B2
АЗ [	6	51	] B3
V <sub>CC</sub> (3.3 V)	7	50	V <sub>CC</sub> (5 V)
A4 [	8	49	] B4
A5 [			B5
A6 [	10	47	] B6
GND [		46	GND
A7 [	12	45	B7
A8 [	13	44	B8
A9 [		43	B9
A10 [	15	42	<b>]</b> B10
A11 [	16	41	B11
A12 [	17	40	B12
GND [	18	39	GND
A13 [	19	38	B13
A14 [	20	37	B14
A15 [	21		B15
V <sub>CC</sub> (3.3 V)	22	35	V <sub>REF</sub>
A16 [	23	34	B16
A17 [	24	33	B17
GND [			GND
A18 [	26		B18
OEBA [	27	30	CLKBA
LEBA [	28	29	CEBA

in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if  $\overline{\text{CEAB}}$  is low and CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB if  $\overline{\text{CEAB}}$  is also low.  $\overline{\text{OEAB}}$  is active low. When  $\overline{\text{OEAB}}$  is low, the outputs are active. When  $\overline{\text{OEAB}}$  is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that for A to B but uses  $\overline{\text{OEBA}}$ , LEBA, CLKBA, and  $\overline{\text{CEBA}}$ .

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54GTL16612 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74GTL16612 is characterized for operation from -40°C to 85°C.

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## SN54GTL16612, SN74GTL16612 18-BIT GTL/LVT UNIVERSAL BUS TRANSCEIVERS

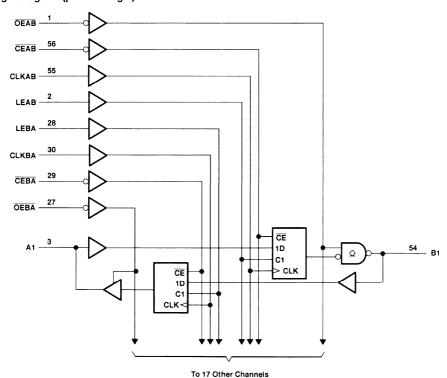
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#### **FUNCTION TABLET**

TOTAL TABLE						
INPUTS					OUTPUT	MODE
CEAB	OEAB	LEAB	CLKAB	Α	В	MODE
Х	Н	Х	X	Х	Z	
L	L	L	Н	X	в <sub>0</sub> ‡	Latched storage of A data
L	L	L	L	X	В <sub>0</sub> §	
X	L	Н	Х	L	L	Transparent
X	L	Н	X	Н	Н	
L	L	L	1	L	L	Cleaked storage of A data
L	L	L	1	Н	н	Clocked storage of A data
Н	L	L	Х	Х	В <sub>0</sub> \$	Clock inhibit

<sup>†</sup> A-to-B data flow is shown: B-to-A data flow is similar but uses  $\overline{\text{OEBA}}$ , LEBA, CLKBA, and  $\overline{\text{CEBA}}$ .

## logic diagram (positive logic)





Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low.

<sup>§</sup> Output level before the indicated steady-state input conditions were established.

## SN54GTL16612, SN74GTL16612 18-BIT GTL/LVT UNIVERSAL BUS TRANSCEIVERS

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub> : 3.3 V –0.5 V to 4.6 V	٧
5 V0.5 V to 7 V	V
nput voltage range, V <sub>I</sub> (see Note 1): A port	v
Tiput voltage range, v <sub>1</sub> (see Note 1). A port	.,
B port	٧
Voltage range applied to any output in the high or	
power-off state, V <sub>O</sub> (see Note 1): A port	٧
B port0.5 V to 4.6 V	
Current into any A-port output in the low state, I <sub>O</sub>	
Current into any B-port output in the low state, IO	
Current into any A-port output in the high state, IO (see Note 2)	
input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air) (see Note 3): DGG package	
DL package	
Operating free-air temperature range, T <sub>A</sub> : SN54GTL16612	
SN74GTL1661240°C to 85°C	
Storage temperature range	С

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This current flows only when the output is in the high state and VO > VCC.
- The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
   For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

#### recommended operating conditions (see Note 4)

			s	N54GTL	16612		SN74GTL	16612	
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
.,	Supply voltage, 3.3 V Supply voltage, 5 V		3.15	3.3	3.45	3.15	3.3	3.45	V
VCC			4.75	5	5.25	4.75	5	5.25	v
VREF	Supply voltage			0.8			0.8		٧
16		B port			V <sub>CC</sub> (3.3 V)			V <sub>CC</sub> (3.3 V)	v
Vi	Input voltage	Except B port			5.5			5.5	\ \
.,	High-level input voltage	B port	V <sub>REF</sub> +50	mV	2	V <sub>REF</sub> +50	mV		V
VIH		Except B port	2	(4) A.		2			ľ
W		B port		35	VREF -50 mV			V <sub>REF</sub> -50 mV	V
VIL	Low-level input voltage	Except B port		.01	0.8			0.8	ľ
lik	Input clamp current		્ર		-18			-18	mA
ЮН	High-level output current	A port			-32	I		-32	mA
1		A port			64			64	
IOL	Low-level output current	B port			40			40	mA
TA	Operating free-air tempera	ature	-55		125	-40		85	°C

NOTE 4: Unused or floating control inputs must be held high or low.



# SN54GTL16612, SN74GTL16612 18-BIT GTL/LVT UNIVERSAL BUS TRANSCEIVERS

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# electrical characteristics over recommended operating free-air temperature range, $V_{REF} = 0.8 \text{ V}$ (unless otherwise noted)

DADAS	JETER	TEST CON	DITIONS	SN5	4GTL16	612	SN7	SN74GTL16612		UNIT		
PARA	METER	TEST CONI	DITIONS	MIN	TYPT	MAX	MIN	TYPT	MAX	ONT		
VIK		V <sub>CC</sub> (3.3 V) = 3.15 V, V <sub>CC</sub> (5 V) = 4.75 V	I <sub>I</sub> = -18 mA			-1.2			-1.2	V		
		V <sub>CC</sub> = MIN to MAX <sup>‡</sup> ,	I <sub>OH</sub> = - 100 μA	V <sub>CC</sub> -	V <sub>CC</sub> - 0.2		V <sub>CC</sub> - 0.2		V <sub>CC</sub> -	0.2		
VOH	A port	$V_{CC}$ (3.3 V) = 3.15 V,	I <sub>OH</sub> = – 8 mA	2.4			2.4			V		
		V <sub>CC</sub> (5 V) = 4.75 V	I <sub>OH</sub> = - 32 mA	2			2					
			I <sub>OL</sub> = 100 μA			0.2			0.2			
	A port	$V_{CC}$ (3.3 V) = 3.15 V,	I <sub>OL</sub> = 16 mA			0.4			0.4			
VOL	Apon	V <sub>CC</sub> (5 V) = 4.75 V	I <sub>OL</sub> = 32 mA			0.5			0.5	v		
VOL			IOL = 64 mA			0.55			0.55			
	B port	$V_{CC}$ (3.3 V) = 3.15 V, $V_{CC}$ (5 V) = 4.75 V	I <sub>OL</sub> = 40 mA			0.4			0.4			
	Control inputs	V <sub>CC</sub> = 0 or MAX <sup>‡</sup> ,	V <sub>I</sub> = 5.5 V			10			10			
			V <sub>I</sub> = 5.5 V			20			20			
l <sub>l</sub>	A port	V <sub>CC</sub> (3.3 V) = 3.45 V, V <sub>CC</sub> (5 V) = 5.25 V	V <sub>I</sub> = V <sub>CC</sub>			1			1	μΑ		
·		VCC (5 V) = 5.25 V	V <sub>I</sub> = 0			-30			-30			
	B port	V <sub>CC</sub> (3.3 V) = 3.45 V,	$V_{I} = V_{CC} (3.3 \text{ V})$		- 4	5		5				
	Броп	V <sub>CC</sub> (5 V) = 5.25 V	V <sub>I</sub> = 0		_45	-5			-5			
loff	A port	V <sub>CC</sub> = 0,	$V_{  }$ or $V_{  } = 0$ to 4.5 V		<u>.</u> C	100			100	μА		
lun, and	A port	V <sub>CC</sub> (3.3 V) = 3.15 V,	V <sub>I</sub> = 0.8 V	75	<u> S</u>		75			μА		
l(hold)	Apon	V <sub>CC</sub> (5 V) = 4.75 V	V <sub>1</sub> = 2 V	-75			-75			, ,		
<sup>I</sup> OZH	A port	$V_{CC}$ (3.3 V) = 3.45 V,	V <sub>O</sub> = 3 V			1			1	ДД		
10ZH	B port	V <sub>CC</sub> (5 V) = 5.25 V	V <sub>O</sub> = 1.2 V			10			10	, , ,		
<sup>I</sup> OZL	A port	$V_{CC}$ (3.3 V) = 3.45 V,	V <sub>O</sub> = 0.5 V			-1			-1	μА		
·OZL	B port	V <sub>CC</sub> (5 V) = 5.25 V	V <sub>O</sub> = 0.4 V			-10			-10			
		$V_{CC}$ (3.3 V) = 3.45 V,	Outputs high			1			1			
I <sub>CC</sub> (3.3 V)	A or B port	$V_{CC}$ (5 V) = 5.25 V, $I_{O}$ = 0,	Outputs low	l		5			5	mA		
		V <sub>I</sub> = V <sub>CC</sub> (3.3 V) or GND	Outputs disabled			1			1			
		V <sub>CC</sub> (3.3 V) = 3.45 V,	Outputs high			120			120			
ICC (5 V)	A or B port	V <sub>CC</sub> (5 V) = 5.25 V, I <sub>O</sub> = 0,	Outputs low			120			120	mA		
		V <sub>I</sub> = V <sub>CC</sub> (5 V) or GND	Outputs disabled			120			120			
ΔI <sub>CC</sub> §		V <sub>CC</sub> (3.3 V) = 3.45 V, A or control inputs at V <sub>CC</sub> ( One input at 2.7 V	V <sub>CC</sub> (5 V) = 5.25 V, (3.3 V) or GND,			1			1	mA		
Ci	Control inputs	V <sub>I</sub> = 3.15 V or 0			3.5			3.5		pF		
C.	A port	V <sub>O</sub> = 3.15 V or 0			12			12		pF		
Cio	B port	Per IEEE Standard 1149.0-	1991			5			5	Pr		

<sup>†</sup> All typical values are at  $V_{CC}$  (3.3 V) = 3.3 V,  $V_{CC}$  (5 V) = 5 V,  $T_A$  = 25°C.



<sup>‡</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>§</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

## SN54GTL16612, SN74GTL16612 18-BIT GTL/LVT UNIVERSAL BUS TRANSCEIVERS

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# timing requirements over recommended ranges of supply voltage and operating free-air temperature, $V_{\mbox{\scriptsize REF}}$ = 0.8 V (unless otherwise noted)

			SN54G	TL16612	SN74G	TL16612	UNIT
1			MIN	MAX	MIN	MAX	UNII
fclock	Clock frequency	The second of th	0	95	0	95	MHz
	Pulse duration	LEAB or LEBA high	3.3		3.3		
¹w	ruise duration	CLKAB or CLKBA high or low	5.6		5.6		ns
		A before CLKAB↑	0.9		0		
l		B before CLKBA↑	3.4		2.5		1
١.	Catus times	A before LEAB↓	1.2		0.4		]
†su	Setup time	B before LEBA↓	1	37	0.9		ns
		CEAB before CLKAB↑	2.1		1		1
		CEBA before CLKBA↑	2.6		2.1		1
		A after CLKAB↑	2.9		2.7		
l		B after CLKBA↑	4.1		0.4		]
	Hald Co.	A after LEAB↓	4.5		3.4		1
th	Hold time	B after LEBA↓	4.3		3.3		ns
		CEAB after CLKAB↑	2		1.5		1
		CEBA after CLKBA↑	0.5		0.4		1

# switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $V_{\text{REF}}$ = 0.8 V (see Figure 1)

	FROM	то	SN5	4GTL16	612	SN7	4GTL16	612	
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYPT	MAX	MIN	TYPT	MAX	UNIT
fmax			95			95			MHz
tPLH .	A	В	1	2.6	3.8	1	2.6	3.8	
tPHL	A	B	1	2.2	4	1	2.2	4	ns
tPLH	LEAB	В	1.8	3.6	5.4	1.8	3.6	5.4	
tPHL	LEAD	P P	1.5	3.3	5.5	1.5	3.3	5.5	ns
t <sub>PLH</sub>	CLKAR	В	1.8	3.7	5.3	1.8	3.7	5.3	
<sup>†</sup> PHL	CLKAB	В	1.5	3.3	5.5	1.5	3.3	5.5	ns
tPLH	2515	В	1.6	3.3	4.7	1.6	3.3	4.7	
tPHL	OEAB	В	1.3	3.2	5.5	1.3	3.2	5.5	ns
t <sub>r</sub>	Transition time, B o	utputs (0.5 V to 1 V)		1.3			1.3		ns
tf	Transition time, B o	utputs (1 V to 0.5 V)		0.5			0.5		ns
t <sub>PLH</sub>	В		2	4.8	6.9	2	4.8	6.9	
t <sub>PHL</sub>	В	A	1.4	3.6	5.1	1.4	3.6	5.1	ns
tPLH			2.1	4.3	6.1	2.1	4.3	6.1	
<sup>t</sup> PHL	LEBA	A	1.9	3.6	5.1	1.9	3.6	5.1	ns
<sup>t</sup> PLH	CLIVDA	Α	2.3	4.5	6.4	2.3	4.5	6.4	
tPHL	CLKBA	^	2.2	4	5.6	2.2	4	5.6	ns
<sup>t</sup> en	OFFIA		1.9	4.7	7.2	1.9	4.7	7.2	
<sup>t</sup> dis	OEBA	A	2.5	4.6	6.9	2.5	4.6	6.9	ns

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC}$  (3.3 V) = 3.3 V,  $V_{CC}$  (5 V) = 5 V,  $T_A$  = 25°C.



#### PARAMETER MEASUREMENT INFORMATION 6 V 1.2 V **500** Ω O Open 25 Ω From Output TEST S1 From Output GND Test Open **Under Test** tPLH/tPHL tPLZ/tPZL **Under Test** 6 V Point Ci = 50 pF 500 Ω GND tPHZ/tPZH $C_1 = 30 pF$ (see Note A) (see Note A) LOAD CIRCUIT FOR B OUTPUTS LOAD CIRCUIT FOR A OUTPUTS - t<sub>w</sub> 3 V Timing Vm V Input Vm V Input nν t<sub>su</sub> **VOLTAGE WAVEFORMS** 3 V **PULSE DURATION** Data (Vm = 1.5 V for A port and 0.8 V for B port) Vm V Vm V Input nν VOLTAGE WAVEFORMS \_ 3 V Input SETUP AND HOLD TIMES (see Note B) (Vm = 1.5 V for A port and 0.8 V for B port) ΛV **t**PLH <sup>t</sup>PHL VOH 3 V Output 0.8 V 0.8 V Output VOL Control 1.5 V 1.5 V (see Note B) **VOLTAGE WAVEFORMS** 0 V PROPAGATION DELAY TIMES tpzL (A port to B port) 3 V Output 1.2 V Input Waveform 1 V<sub>OL</sub> + 0.3 V 087 (see Note B) S1 at 6 V οv (see Note C) <sup>t</sup>PHZ tPZH **tPHL** Output ۷он Vон V<sub>OH</sub> - 0.3 V

NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

1.5 V

**VOLTAGE WAVEFORMS** PROPAGATION DELAY TIMES

(B port to A port)

Output

B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>f</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.

Waveform 2

(see Note C)

**VOLTAGE WAVEFORMS** 

**ENABLE AND DISABLE TIMES** (A port)

 $\approx$  0 V

- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

VOL



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- Translates Between GTL Signal Levels and LVTTL or 5-V TTL Signal Levels
- Members of the Texas Instruments Widebus™ Family
- Supports Mixed-Mode Signal Operation on A Port
- Universal Bus Transceiver (UBT™)
   Combines D-Type Latches and D-Type
   Flip-Flops With Qualified Storage Enable
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors on A Port
- Flow-Through Architecture Optimizes PCB Layout
- Package Options Include Plastic Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Ceramic Flat (WD) Packages

#### description

These 17-bit registered bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes. The 'GTL16616 provides for a copy of CLKAB at GTL logic levels (CLKOUT) and also provides a conversion of the GTL clock to a TTL environment (CLKIN).

The B port operates at GTL levels while the A port and control pins are compatible with LVCMOS, LVTTL, or 5-V TTL logic levels.

Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and

SN54GTL16616 . . . WD PACKAGE SN74GTL16616 . . . DGG OR DL PACKAGE (TOP VIEW)

		_	
OEAB [	I₁ ∪	56	CEAB
LEAB [			CLKAB
A1 [	3	54	B1
GND [	4	53	GND
A2 [	5		B2
A3 [		51	B3
V <sub>CC</sub> (3.3 V) [	7		V <sub>CC</sub> (5 V)
A4 [	8		B4
A5 [		48	B5
A6 [			B6
GND [			GND
A7 [			B7
A8 [			B8
A9 [			B9
A10 [			B10
A11 [			B11
A12 [			B12
GND [			GND
A13 [			B13
A14 [			B14
A15 [			B15
V <sub>CC</sub> (3.3 V)			V <sub>REF</sub>
A16 [			B16
A17 [			B17
GND [			GND
CLKIN [			CLKOUT
OEBA [			CLKBA
LEBA [	28	29	CEBA

CLKBA) inputs. The clock or latch-enable can be controlled by the clock-enable ( $\overline{CEAB}$  and  $\overline{CEBA}$ ) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if  $\overline{CEAB}$  is low and CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB if  $\overline{CEAB}$  is also low.  $\overline{OEAB}$  is active low. When  $\overline{OEAB}$  is low, the outputs are active. When  $\overline{OEAB}$  is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that of A to B but uses  $\overline{OEAB}$ , LEBA, CLKBA, and  $\overline{CEBA}$ .

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74GTL16616 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54GTL16616 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74GTL16616 is characterized for operation from -40°C to 85°C.

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#### FUNCTION TABLET

		INPUTS			OUTPUT	MODE
CEAB	OEAB	LEAB	CLKAB	Α	В	MODE
X	Н	Х	X	X	Z	
L	L	L	H or L	Χ	в <sub>0</sub> ‡	Latched storage of A data
L	L	L	H or L	Χ	В <sub>0</sub> §	
×	L	Н	X	L	L	Transparent
×	L	н	X	Н	н	Hansparent
L	L	L	1	L	L	Clocked storage of A data
L	L	L	1	Н	н	Glocked Storage of A data
Н	L	L	X	Х	B <sub>0</sub> §	Clock inhibit

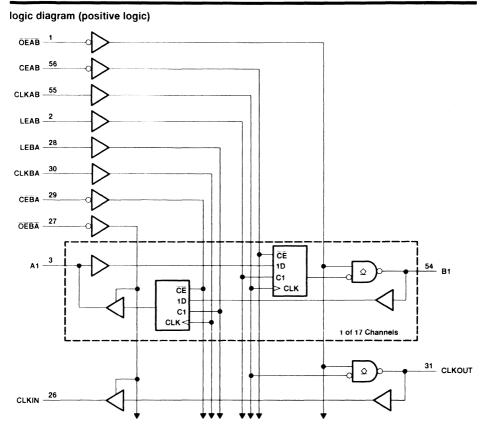
<sup>†</sup> A-to-B data flow is shown: B-to-A data flow is similar but uses OEBA, LEBA, CLKBA, and CEBA.



<sup>‡</sup> Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low.

<sup>§</sup> Output level before the indicated steady-state input conditions were established.

# SN54GTL16616, SN74GTL16616 17-BIT GTL/LVT UNIVERSAL BUS TRANSCEIVERS WITH BUFFERED CLOCK OUTPUTS SCBS481A - JUNE 1994 - REVISED AUGUST 1994





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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub> : 3.3 V	-0.5 V to 4.6 V
5 V	0.5 V to / V
Input voltage range, V <sub>I</sub> (see Note 1): A port	0.5 V to 7 V
B port	. −0.5 V to 4.6 V
Voltage range applied to any output in the high or	
power-off state, VO (see Note 1): A port	0.5 V to 7 V
B port	-0.5 V to 4.6 V
Current into any A-port output in the low state, I <sub>O</sub>	128 mA
Current into any B-port output in the low state, IO	80 mA
Current into any A-port output in the high state, IO (see Note 2)	64 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–50 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air) (see Note 3): DGG package	1 W
DL package	1.4 W
Storage temperature range	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This current will flow only when the output is in the high state and  $V_{O} > V_{CC}$ .
- The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
  For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology
  Data Book, literature number SCBD002B.

#### recommended operating conditions (see Note 4)

			8	N54GTL	16616		N74GTL	16616	
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
V	Supply voltage, 3.3 V Supply voltage, 5 V		3.15	3.3	3.45	3.15	3.3	3.45	V
VCC			Supply voltage, 5 V 4.75	Supply voltage, 5 V		5	5.25	4.75	5
VREF	Supply voltage			0.8			0.8		V
VI	Input voltage	B port			V <sub>CC</sub> (3.3 V)			V <sub>CC</sub> (3.3 V)	v
۷Į	input voltage	Except B port			5.5			5.5	)
Vivi	High-level input voltage	B port	VREF +50	mV		VREF +50	mV		V
VIH		Except B port	2	- A.S.		2			ľ
Vii	Low-level input voltage	B port		-32	VREF -50 mV			VREF -50 mV	V
VIL	Low-level input voltage	Except B port		ं	0.8			0.8	ľ
lik	Input clamp current				-18			-18	mA
ЮН	High-level output current	A port			-32			-32	mA
lo:	Low-level output current	A port			64			64	
OL	Low-level output current	B port			40			40	mA
TA	Operating free-air tempera	ature	-55		125	-40		85	°C

NOTE 4: Unused or floating control inputs must be held high or low.



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# electrical characteristics over recommended operating free-air temperature range, $V_{REF} = 0.8 \text{ V}$ (unless otherwise noted)

DADA	METER	TEST CON	DITIONS	SN5	4GTL16	616	SN7	4GTL16	616	UNIT
PARA	MEIER	TEST CON	DITIONS	MIN	TYPT	MAX	MIN	TYP	MAX	UNII
VIK		$V_{CC}$ (3.3 V) = 3.15 V, $V_{CC}$ (5 V) = 4.75 V	I <sub>I</sub> = -18 mA			~1.2			-1.2	V
		VCC = MIN to MAX‡,	I <sub>OH</sub> = -100 μA	VCC-	0.2		VCC-	0.2		
V <sub>OH</sub>	A port	V <sub>CC</sub> (3.3 V) = 3.15 V,	I <sub>OH</sub> = -8 mA	2.4			2.4			V
		V <sub>CC</sub> (5 V) = 4.75 V	I <sub>OH</sub> = - 32 mA	2			2			
			I <sub>OL</sub> = 100 μA			0.2			0.2	
	A port	$V_{CC}$ (3.3 V) = 3.15 V,	I <sub>OL</sub> = 16 mA			0.4			0.4	
VOL	l Pon	V <sub>CC</sub> (5 V) = 4.75 V	IOL = 32 mA	1		0.5			0.5	v
- OL			IOL = 64 mA	1		0.55			0.55	
	B port	$V_{CC} (3.3 \text{ V}) = 3.15 \text{ V},$ $V_{CC} (5 \text{ V}) = 4.75 \text{ V}$	I <sub>OL</sub> = 40 mA			0.4			0.4	
	Control inputs	V <sub>CC</sub> = 0 or MAX <sup>‡</sup> ,	V <sub>1</sub> = 5.5 V		10 20				10	
			V <sub>I</sub> = 5.5 V	1			20			
l <sub>l</sub>	A port	V <sub>CC</sub> (3.3 V) = 3.45 V, V <sub>CC</sub> (5 V) = 5.25 V	VI = VCC			1			1	μА
		V(( (5 V) = 5.25 V	V <sub>1</sub> = 0	1		-30			-30	
	B port	V <sub>CC</sub> (3.3 V) = 3.45 V,	$V_{I} = V_{CC} (3.3 \text{ V})$	1	5			5		
	B port	V <sub>CC</sub> (5 V) = 5.25 V	V <sub>1</sub> = 0			-5			-5	
loff	A port	V <sub>CC</sub> = 0,	$V_1$ or $V_0 = 0$ to 4.5 V		- 4	100			100	μΑ
l(hold)	A port	$V_{CC}$ (3.3 V) = 3.15 V,	V <sub>I</sub> = 0.8 V	75			75			μА
'I(noid)	71 port	V <sub>CC</sub> (5 V) = 4.75 V	V <sub>1</sub> = 2 V	-75	<u> </u>		-75			μ.,
lozн	A port	V <sub>CC</sub> (3.3 V) = 3.45 V.	V <sub>O</sub> = 3 V	3	·	1			1	μА
-0211	B port	V <sub>CC</sub> (5 V) = 5.25 V	V <sub>O</sub> = 1.2 V			10			10	
<sup>I</sup> OZL	A port	$V_{CC}$ (3.3 V) = 3.45 V,	V <sub>O</sub> = 0.5 V	<u> </u>		-1			-1	μА
	B port	V <sub>CC</sub> (5 V) = 5.25 V	V <sub>O</sub> = 0.4 V	<u> </u>		-10			-10	
		$V_{CC}$ (3.3 V) = 3.45 V,	Outputs high			1			1	
I <sub>CC</sub> (3.3 V)	A or B port	$V_{CC}$ (5 V) = 5.25 V, $I_{C}$ = 0,	Outputs low			5			5	mA
		$V_I = V_{CC}$ (3.3 V) or GND	Outputs disabled			1			1	
		V <sub>CC</sub> (3.3 V) = 3.45 V,	Outputs high			120			120	
ICC (5 V)	A or B port	V <sub>CC</sub> (5 V) = 5.25 V,	Outputs low	1		120			120	mA
	İ	$I_O = 0$ , $V_I = V_{CC}$ (5 V) or GND	Outputs disabled			120			120	
ΔICC§		V <sub>CC</sub> (3.3 V) = 3.45 V, A or control inputs at V <sub>CC</sub> One input at 2.7 V	V <sub>CC</sub> (5 V) = 5.25 V, (3.3 V) or GND,			1			1	mA
Ci	Control inputs	V <sub>I</sub> = 3.15 V or 0			3.5			3.5		рF
Cio	A port	V <sub>O</sub> = 3.15 V or 0			12			12		- F
~10	B port	Per IEEE 1194.0-1991				5			5	ρF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC}$  (3.3 V) = 3.3 V,  $V_{CC}$  (5 V) = 5 V,  $T_{A}$  = 25°C.



For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>§</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature,  $V_{\text{REF}} = 0.8 \text{ V}$  (unless otherwise noted)

			SN54G	TL16616	SN74G	TL16616	UNIT
			MIN	MAX	MIN	MAX	UNII
fclock	Clock frequency		0	95	0	95	MHz
	Pulse duration	LEAB or LEBA high	3.3	•	3.3		ns
tw	ruise duration	CLKAB or CLKBA high or low	5.5		5.5		115
		A before CLKAB↑	1.1		1.1		
	t <sub>Su</sub> Setup time	B before CLKBA↑	2.6		2.6		
		A before LEAB↓	0		0		]
<sup>t</sup> su		B before LEBA↓	1	Q <sup>2</sup>	1		ns
		CEAB before CLKAB↑	1.8		1.8		1
		CEBA before CLKBA↑	2.1		2.1		
		A after CLKAB↑	1,6		1.6		
		B after CLKBA↑	0.2		0.2		1
	11.112	A after LEAB↓	4.3		4.3		]
th	Hold time	B after LEBA↓	2.8		2.8		ns
		CEAB after CLKAB↑	0.8		0.8		1
		CEBA after CLKBA↑	0.7		0.7		]

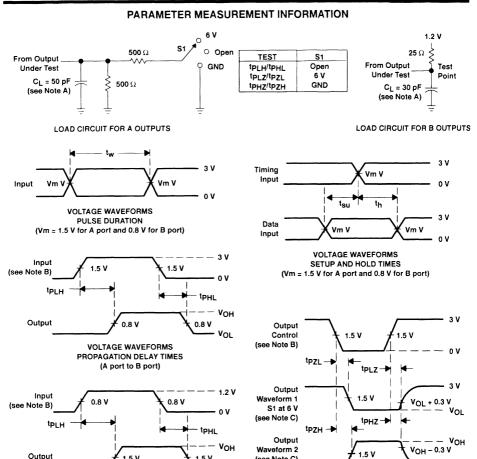
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# switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $V_{\text{REF}}$ = 0.8 V (see Figure 1)

PARAMETER	FROM	то	SNS	4GTL16	616	SN7	4GTL16	616	UNIT
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYPT	MAX	MIN	TYPT	MAX	UNII
fmax			95			95			MHz
t <sub>PLH</sub>	А	В	1	2.5	3.8	1	2.5	3.8	ns
t <sub>PHL</sub>		B	1	2	3.8	1	2	3.8	115
t <sub>PLH</sub>	LEAB	В	1.5	3.4	5.1	1.5	3.4	5 1	ns
<sup>t</sup> PHL	LEAD	P	1.4	3.2	5.1	1.4	3.2	5.1	115
<sup>t</sup> PLH	CLKAB	В	1.5	3.6	5	1.5	3.6	5	ns
<sup>t</sup> PHL	CERAB		1.4	4.1	5	1.4	4.1	5	113
tPLH	CLKAB	CLKOUT	3.4	6	7.7	3.4	6	7.7	ns
tphL	CLNAB	CEROUT	4.3	7.4	10.4	4.3	7.4	10.4	115
<sup>t</sup> PLH	ŌĒĀB	В	1.3	3.2	5	1.3	3.2	5	ns
<sup>t</sup> PHL	OEAB	В	1.1	3.1	5	1.1	3.1	5	115
t <sub>r</sub>	Transition time, B o	utputs (0.5 V to 1 V)		1.2			1.2		ns
tf	Transition time, B o	utputs (1 V to 0.5 V)	3	0.7			0.7		ns
tPLH	В	A	2.1	4.4	6.5	2.1	4.4	6.5	ns
<sup>t</sup> PHL	В	Ŷ.	1.3	3.3	4.8	1.3	3.3	4.8	113
tPLH	LEBA	А	1.7	3.9	6	1.7	3.9	6	ns
<sup>t</sup> PHL	LLDA		1.3	3.3	4.6	1.3	3.3	4.6	115
tPLH	CLKBA	А	1.7	4.1	6.3	1.7	4.1	6.3	ns
<sup>t</sup> PHL	CLRDA	^	1.4	3.6	5.3	1.4	3.6	5.3	115
<sup>†</sup> PLH	CLKOUT	CLKIN	6.5	10.5	14.3	6.5	10.5	14.3	ns
<sup>t</sup> PHL	CEROOT	CERIN	5.1	8.8	11.8	5.1	8.8	11.8	115
<sup>t</sup> en	ŌĒBĀ	A	1.8	4.7	6.9	1.8	4.7	6.9	ns
<sup>†</sup> dis	OLDA	1 ^	2	4.7	6.7	2	4.7	6.7	115

<sup>†</sup> All typical values are at V<sub>CC</sub> (3.3 V) = 3.3 V, V<sub>CC</sub> (5 V) = 5 V, T<sub>A</sub> = 25°C.

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NOTES: A. CL includes probe and jig capacitance.

1.5 V

**VOLTAGE WAVEFORMS** PROPAGATION DELAY TIMES

(B port to A port)

B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_{\Omega} = 50 \Omega$ ,  $t_r \leq 2.5$  ns.  $t_f \leq 2.5$  ns.

(see Note C)

VOLTAGE WAVEFORMS

ENABLE AND DISABLE TIMES

(A port)

- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms



ETL Enhanced Transceiver Logic	1
BTL Backplane Transceiver Logic	2
GTL Gunning Transceiver Logic	3
ABT/CBT 25-Ω Incident-Wave Switching Drivers	4
Mechanical Data	5

Today designers are often faced with the problem of bus interface circuits having insufficient drive capability when driving low-impedance bus lines. Transmission lines with a characteristic impedance of less than 30 ohms are no longer a rarity (mainframe computers; switching systems; industrial control systems). If the necessary output current cannot be provided the result will generally be a reduction in system speed.

As the line impedance can hardly by influenced, the driver needs to provide sufficient drive capability. In other words, the driver output needs to provide a sufficiently high amount of current to switch the bus or the line directly from one logic state to the other (incident wave switching, IWS). Otherwise, it takes several wave reflections until the line signal level reaches the desired logic level.

To support IWS on highly-loaded lines, TI has developed several BiCMOS functions, designated SN74BCT25xxx, which offer an extended output drive of  $I_0I - 188$  mA and  $I_0h = 80$  mA, which is sufficient for reliable operation of lines with impedances down to 25 ohms.

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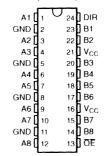
- State-of-the-Art EPIC-IIB M BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Designed to Facilitate Incident-Wave Switching for Line Impedances of 25 Ω or Greater
- Distributed V<sub>CC</sub> and GND Pins Minimize Noise Generated by the Simultaneous Switching of Outputs
- Bus-Hold Inputs Eliminate the Need for External Pullup Resistors
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

#### description

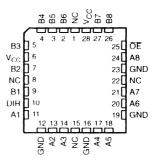
The 'ABT25245 is a 25- $\Omega$  octal bus transceiver designed for asynchronous communication between data buses. It improves both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented transceivers

The device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable (OE) input can disable the device so that both buses are effectively isolated.

SN54ABT25245...JT PACKAGE SN74ABT25245...DW OR NT PACKAGE (TOP VIEW)



SN54ABT25245 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

This transceiver is capable of sinking 188 mA of  $I_{OL}$  current, which facilitates switching 25- $\Omega$  transmission lines on the incident wave. The distributed  $V_{CC}$  and GND pins minimize switching noise for more reliable system operation.

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{\overline{CC}}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT25245 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT25245 is characterized for operation from –40°C to 85°C.

EPIC-IIB is a trademark of Texas Instruments Incorporated

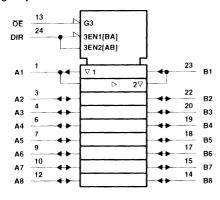
# SN54ABT25245, SN74ABT25245 25- $\Omega$ OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

JUNE 1992 - REVISED FEBRUARY 1993

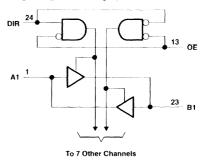
#### **FUNCTION TABLE**

INP	UTS	OPERATION
ŌĒ	DIR	OFERATION
L	L	B data to A bus
L	Н	A data to B bus
Н	X	Isolation

## logic symbol†



#### logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages

# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, V <sub>O</sub>	0.5 V to 5.5 V
Voltage range applied to any output in the high state, V <sub>O</sub>	0.5 V to V <sub>CC</sub>
Input clamp current, $I_{IK}(V_1 < 0)$	
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Current into any output in the low state, Io: SN54ABT25245 (A port)	250 mA
SN54ABT25245 (B port)	96 mA
SN74ABT25245 (A port)	
SN74ABT25245 (B port)	128 mA
Operating free-air temperature range: SN54ABT25245	55°C to 125°C
SN74ABT25245	40°C to 85°C
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air): DW package	1 W
NT package	1.3 W
Storage temperature range	65°C to 150°C

<sup>‡</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed



<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

# SN54ABT25245, SN74ABT25245 25-\(\Omega\) OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS JUNE 1992 REVISED FEBRUARY 1993

## recommended operating conditions (see Note 2)

				SN54AB	T25245	SN74AB	T25245	UNIT	
				MIN	MAX	MIN	MAX	AX	
Vcc	Supply voltage			4.5	5.5	4.5	5.5	V	
VIH	High-level input voltage			2		2		V	
VIL	Low-level input voltage				₹0.8		0.8	٧	
VI	Input voltage			0	₩ <sub>CC</sub>	0	V <sub>CC</sub>	٧	
l <sub>ik</sub>	Input clamp current			4	-18		-18	mA	
	High-level output current		A ports	~	- 53		-80	mA	
ЮН	riigh-ieveroutput current		B ports	30	-24		-32	IIIA	
,	Low-level output current		A ports	S	125		188	mA	
<sup>†</sup> OI	Cow-rever output current		B ports	Q	48		64	mA	
11/1v	Input transition rise or fall rate	Outputs anabled	Control inputs		4		4	n= 0/	
.10.10	input transition use of fall fate	Outputs enabled	A or B ports		10		10	ns/V	
TA	Operating free-air temperature			-55	125	-40	85	°C	

NOTE 2 Unused or floating pins (input or I/O) must be held high or low.

# SN54ABT25245, SN74ABT25245 25- $\Omega$ OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

		ER TEST CONDITIONS		SN5	4ABT2	245	SN74ABT25245				
P	ARAMETER		TEST CONDITION	15	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V.	I <sub>I</sub> = -18 mA				-1.2			-1.2	٧
		$V_{CC} = 4.75 \text{ V}.$	$I_{OH} = -3 \text{ mA}$					2.7			
	A ports	$V_{\rm CC} = 4.5 \text{ V}.$	I <sub>OH</sub> = -53 mA		2						
		$V_{\rm CC} = 4.5 \text{ V},$	$I_{OH} = -80 \text{ mA}$					2.4			
$V_{OH}$		$V_{CC} = 4.5 \text{ V}.$	$I_{OH} = -3 \text{ mA}$		2.5			2.5			V
	B ports	V <sub>CC</sub> = 5 V.	I <sub>OH</sub> = - 3 mA		3			3			
	l	$V_{CC} = 4.5 \text{ V}.$	$I_{OH} = -32 \text{ mA}$					2			
		$V_{CC} = 4.5 \text{ V}.$	I <sub>OL</sub> = 94 mA				0.55			0.55	
	A ports	$V_{CC} = 4.5 \text{ V}.$	$I_{OL} = 125 \text{ mA}$				8.0				
$V_{OL}$		$V_{\rm CC}$ = 4.5 V.	I <sub>OL</sub> = 188 mA							0.7	V
	B ports	$V_{\rm CC} = 4.5 \text{ V},$	I <sub>OL</sub> = 55 mA				±1 ±100				
	B ports	$V_{\rm CC} = 4.5 \text{ V},$	I <sub>OL</sub> = 64 mA				w.			0.55	
1.	Control inputs	V55V	V <sub>I</sub> = V <sub>CC</sub> or GND			Ž.	±1			±1	μА
11	A or B ports	VCC = 3:3 V.	1 - 100 or and		100 -100c		±100			±100	μА
	A or B ports	$V_{\rm CC} = 4.5 \text{ V},$	$V_I = 0.8 V$		100	3		100			μА
hold	A or B ports	$V_{CC} = 4.5 \text{ V},$			-1000	<u> </u>		-100			μΛ
l <sub>OZH</sub> t		$V_{CC} = 5.5 \text{ V},$	$V_0 = 2.7 \text{ V}$		Q*		50			50	μA
l <sub>OZL</sub> ‡		$V_{\rm CC} = 5.5 \text{ V},$	V <sub>O</sub> = 0.5 V				-50			-50	μΑ
loff		V <sub>CC</sub> = 0,	$V_I$ or $V_O \le 4.5 \text{ V}$				±500			±100	μA
I <sub>CEX</sub>		$V_{CC} = 5.5 \text{ V},$	V <sub>O</sub> = 5.5 V	Outputs high			50			50	μА
lo <sup>§</sup>	B ports	$V_{CC} = 5.5 \text{ V},$	$V_0 = 2.5 \text{ V}$		-50		-210	-50		-210	mA
			0.4.1.	Outputs high			500			500	μA
loc		$V_{CC} = 5.5 \text{ V}$ , $V_{I} = V_{CC} \text{ or GN}$	Outputs open.	Outputs low			20			20	mA
		1		Outputs disabled			500			500	μА
∆l <sub>CC</sub> ¶		V <sub>CC</sub> = 5.5 V. Other inputs at	One input at 3.4 V, V <sub>CC</sub> or GND				1			1	mA
Ci	Control inputs	V <sub>CC</sub> = 5 V,	V <sub>I</sub> =V <sub>CC</sub> or GND			4			4		pF
Cio	A or B ports		V <sub>O</sub> ≈V <sub>CC</sub> or GND			11.5			11.5		pF

<sup>&</sup>lt;sup>†</sup> All typical values are at V<sub>CC</sub> ≈ 5 V, T<sub>A</sub> = 25°C.



 $<sup>^{\</sup>dagger}$  For I/O ports, the parameters  $I_{IH}$  and  $I_{IL}$  include the off-state output current.

<sup>§</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second

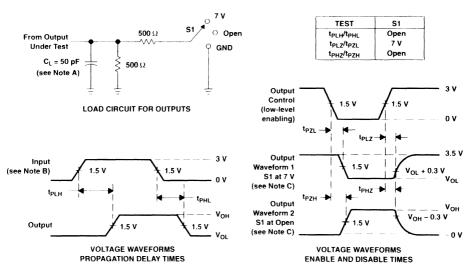
<sup>¶</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>0</sub>	CC = 5 V		SN54ABT	25245	SN74AB	Г25245	UNIT
	(1147-01)	(001701)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
telH	A or B	B or A	1	2.3	3.5	1	\$ 4	1	3.9	
tpHL	AOFB	BOLA	1	2.4	3.5	1 0	4.5	1	4.3	ns
t <sub>PZH</sub>	ŌĒ	A == D	1.5	3.7	5.4	1.9	6.8	1.5	6.5	
tezu	OE.	A or B	1.4	4	5.8	28	7.1	1.4	6.8	ns
t <sub>PHZ</sub>	ŌĒ	A D	2	4.3	6.1	Q 2	7.4	2	7.2	
tplz	OE.	A or B	2	3.9	5.8	<b>Q</b> 2	7.3	2	6.4	ns

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C. includes probe and jig capacitance

- B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>0</sub> = 50 Ω, t<sub>f</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns,
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



## SN54BCT25244, SN74BCT25244 25-\(\Omega\) BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS064A-D3533, JUNE 1990-REVISED NOVEMBER 1991

- State-of-the-Art BiCMOS Design Significantly Reduces I<sub>CCZ</sub>
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Designed to Facilitate Incident-Wave Switching for Line Impedances of 25  $\Omega$  or Greater
- Distributed V<sub>CC</sub> and GND Pins Minimize Noise Generated by the Simultaneous Switching of Outputs
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

#### description

These  $25-\Omega$  octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

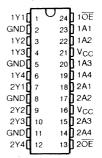
These buffers are capable of sinking a 188-mA  $I_{OL}$ , which facilitates switching 25- $\Omega$  transmission lines on the incident wave. The distributed  $V_{CC}$  and GND pins minimize switching noise for more reliable system operation.

When the output-enable  $(1\overline{OE} \text{ and } 2\overline{OE})$  inputs are low, the device transmits data from the A inputs to the Y outputs. When  $1\overline{OE}$  and  $2\overline{OE}$  are high, the outputs are in the high-impedance state.

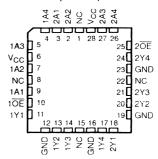
The SN54BCT25244 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74BCT25244 is characterized for operation from 0°C to 70°C.

ifications per the terms of Texas Instruments standard warranty. duction processing does not necessarily include testing of all

#### SN54BCT25244 . . . JT PACKAGE SN74BCT25244 . . . DW OR NT PACKAGE (TOP VIEW)



# SN54BCT25244 ... FK PACKAGE (TOP VIEW)



NC - No internal connection

#### FUNCTION TABLE (EACH BUFFER/DRIVER)

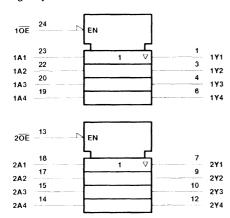
,		
INPL	JTS	OUTPUT
ŌĒ	A	Y
н	Х	z
L	L	L
L	Н	н



# SN54BCT25244, SN74BCT25244 $25-\Omega$ BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

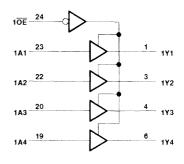
SCBS064A=D3533 JUNE 1990=REVISED NOVEMBER 1991

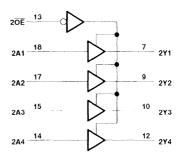
## logic symbol<sup>†</sup>



<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)





# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V <sub>CC</sub>		–0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)		
Voltage applied to any output in the dis	abled or power-off state, VO	0.5 V to 5.5 V
Voltage applied to any output in the hig	<sub>i</sub> h state, V <sub>○</sub>	0.5 V to V <sub>CC</sub>
Input clamp current, $I_{1K}$ ( $V_1 < 0$ )		–30 mA
Current into any output in the low state	, IO: SN54BCT25244	250 mA
	SN74BCT25244	376 mA
Operating free-air temperature range:	SN54BCT25244	–55°C to 125°C
	SN74BCT25244	0°C to 70°C
Storage temperature range		–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

Pin numbers shown are for DW, JT, and NT packages



# SN54BCT25244, SN74BCT25244 25-Ω BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS064A-D3533, JUNE 1990-REVISED NOVEMBER 1991

## recommended operating conditions (see Note 2)

		SN	54BCT2	5244	SN7	UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX	UNII
VCC	Supply voltage	4.5	5	<b>3</b> 5.5	4.5	5	5.5	٧
VIH	High-level input voltage	2		W.	2			٧
VIL	Low-level input voltage		Q.	0.8			0.8	V
ЧK	Input clamp current		4	18			-18	mA
ЮН	High-level output current		S	-53			80	mA
lol	Low-level output current	Q	3	125			188	mA
TA	Operating free-air temperature	-55		125	0		70	°C

NOTE 2: Unused or floating inputs must be held high or low.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54BCT25	244	SN	74BCT2	5244	UNIT
PAHAMETER	TEST CONDITIONS	MIN TYPT	MAX	MIN	TYP	MAX	UNII
VIK	$V_{CC} = 4.5 \text{ V}, \qquad I_{\parallel} = -18 \text{ mA}$		-1.2			-1.2	٧
	V <sub>CC</sub> = 4.75 V, I <sub>OH</sub> = -3 mA			2.7			
v <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -53 mA	2					V
	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -80 mA			2			
	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 94 mA	0.38	0.55		0.42	0.55	
VOL	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 125 mA		0.8				٧
	V <sub>CC</sub> - 4.5 V, I <sub>OL</sub> - 188 mA		3			0.7	
lı .	$V_{CC} = 5.5 \text{ V}.$ $V_{\parallel} = 5.5 \text{ V}$		0.1			0.1	mA
ΙΗ	$V_{CC} = 5.5 \text{ V}, \qquad V_{i} = 2.7 \text{ V}$	1	20			20	μА
lιL	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0.5 V	200	-0.6			-0.6	mA
<sup>I</sup> OZH	$V_{CC} = 5.5 \text{ V},  V_{O} = 2.7 \text{ V}$	, S	50			50	μА
lozl	$V_{CC} = 5.5 \text{ V},  V_{O} = 0.5 \text{ V}$	₹	-50			-50	μА
<sup>I</sup> CCL	V <sub>CC</sub> = 5.5 V, Outputs open	90	119		90	119	mA
ГССН	V <sub>CC</sub> = 5.5 V, Outputs open	59	78		59	78	mA
lccz	V <sub>CC</sub> = 5.5 V, Outputs open	7	11		7	11	mA
C <sub>I</sub>	V <sub>CC</sub> = 5 V, V <sub>I</sub> = V <sub>CC</sub> or GND	5.5			5.5		pF
Co	V <sub>CC</sub> = 5 V, V <sub>O</sub> = V <sub>CC</sub> or GND	17			17		pF

 $<sup>^\</sup>dagger$  All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

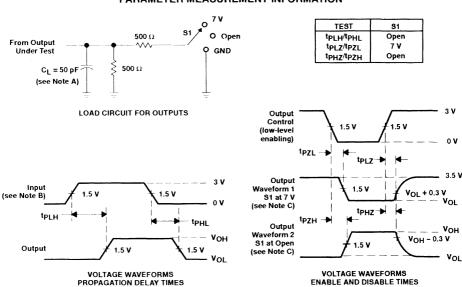


SCBS064A-D3533, JUNE 1990-REVISED NOVEMBER 1991

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50 \text{ pF}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	TO (OUTPUT)	V <sub>t</sub>	CC = 5 A = 25°	<b>V</b> ,	SN54B	CT25244	SN74B	CT25244	UNIT
	(INPUT)	(001701)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
†PLH			1	3.2	4.9	1	530	1	5.5	
tpHL tpHL	A	Y	2	4	5.6	2	6.3	2	6	ns
t <sub>P</sub> ZH			3.2	5.6	8.5	3.2	9.7	3.2	9.3	
†PZL	ŌĒ	Y	3.7	6.3	9.2	3.7	10.4	3.7	10.2	ns
t <sub>PHZ</sub>		· ·	1.6	3.6	5.5	180	6.5	1.6	6.3	200
tPLZ	ŌĒ	· ·	3.1	5.3	7.8	<b>2</b> €.1	9.5	3.1	8.4	ns

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_f \leq$  2.5 ns,  $t_f \leq$  2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



SCBS051 - TI0220 - D3514. MAY 1990 - REVISED SEPTEMBER 1990

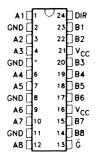
- State-of-the-Art BICMOS Design Significantly Reduces ICCZ
- Designed to Facilitate Incident Wave Switching for Line Impedances of 25-Ohm or Greater
- Distributed V<sub>CC</sub> and GND Pins Minimize Noise Generated by the Simultaneous Switching of Outputs
- Data Flow-Through Pinout (All Inputs on Opposite Side from Outputs)
- ESD Protection Exceeds 2000 V per Mil-Std-883C Method 3015
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

#### description

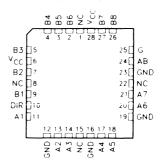
These 25-ohm octal bus transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input G can be used to disable the device so that the buses are effectively isolated.

These transceivers are capable of sinking 188 mA of IOL current (A port), which facilitates switching 25-ohm transmission lines on the incident wave. They are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented transceivers. The distributed VCC and GND pins minimize the noise generated by the simultaneous switching of the outputs.

#### SN54BCT25245 ... JT PACKAGE SN74BCT25245 ... DW or NT PACKAGE (TOP VIEW)



#### SN54BCT25245 ... FK PACKAGE (TOP VIEW)



NC-No internal connection

The SN54BCT25245 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74BCT25245 is characterized for operation from 0°C to 70°C.

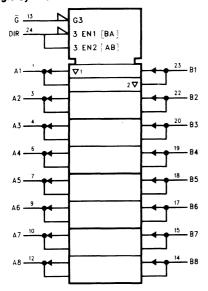


D3514, MAY 1990 - REVISED SEPTEMBER 1990 - TI0220 - SCBS051

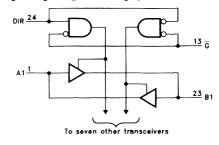
#### **FUNCTION TABLE**

	ENABL	E INPUTS	OPERATION
	Ğ DIR		'BCT25245
-	L	L	B Data to A Bus
	L	н	A Data to B Bus
	н	x	Isolation

## logic symbol<sup>†</sup>



logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SCBS051 - TI0220 - D3514. MAY 1990 - REVISED SEPTEMBER 1990

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)† Supply voltage range, V<sub>CC</sub> .... – 0.5 V to 7 V Input voltage range (see Note 1): Control Inputs ...... - 0.5 V to 7 V Voltage applied to any output in the disabled or power-off state ...... -0.5 V to 5.5 V Voltage applied to any output in the high state (B port) ...... - 0.5 V to V<sub>CC</sub> Input clamp current ..... Operating free-air temperature range: SN54BCT25245 -- 55°C to 125°C SN74BCT25245 ..... 0°C to 70°C Storage temperature range .....

#### recommended operating conditions

		1,484	'54BCT25245			'74BCT25245			
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
VCC	Supply voltage	4.5	5	5.5	4.5	5	5.5	V	
VIН	High-level input voltage		2			2			٧
VIL	Low-level input voltage				0.8			0.8	٧
ЧK	Input clamp current				- 18			- 18	mA
Юн	High-level output current	A1-A8			- 53			- 80	mA
		B1-B8			- 3			-3	
İOL		A1-A8			125			188	
	Low-level output current	B1-B8			20			24	mA
TA	Operating free-air temperature		- 55		125	0		70	°C



<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

D3514, MAY 1990 - REVISED SEPTEMBER 1990 - TI0220 - SCBS051

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED		TEST COUNTIONS	'54	'54BCT25245			'74BCT25245		
P	ARAMETER	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
VIK		V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA			- 1.2			- 1.2	٧
		V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -53 mA	2						
V	Any A	$V_{CC} = 4.5 \text{ V},  I_{OH} = -80 \text{ mA}$				2			٧
۷ОН		$V_{CC} = 4.75 \text{ V},  I_{OH} = -3 \text{ mA}$				2.7			. v
	Any B	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA	2.4	3.3		2.4	3.3		
		V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 94 mA		0.38	0.55		0.42	0.55	
	Any A	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 125 mA			0.8				
VOL	1	$V_{CC} = 4.5  \text{V},  I_{OL} = 188  \text{mA}$						0.7	V
	Any B	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 20 mA		0.3	0.5				
		V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 24 mA					0.35	0.5	
1.	A and B	V <sub>CC</sub> = 5.5 V, V <sub>1</sub> = 5.5 V			0.25			0.25	mA
IJ	DIR and G	$V_{CC} = 5.5  V,  V_{I} = 5.5  V$			0.1			0.1	mA
1+	A and B	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 2.7 V			70			70	
ηΗ‡	DIR and G	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 2.7 V			20			20	μА
i +	A and B	$V_{CC} = 5.5  V,  V_1 = 0.5  V$			- 0.6			- 0.6	mA
IIL‡	DIR and G	$V_{CC} = 5.5  V,  V_1 = 0.5  V$			- 0.6			- 0.6	mA
los <sup>§</sup>	B port only¶	$V_{CC} = 5.5  V,  V_{O} = 0$	- 60		- 150	- 60		- 150	mA
1	A to B	V <sub>CC</sub> = 5.5 V		36	46		36	46	mA
ICCH	B to A			63	77		63	77	mA
1	A to B	V <sub>CC</sub> = 5.5 V		48	60		48	60	mA
ICCL	B to A			95	115		95	115	mA
ICCZ		V <sub>CC</sub> = 5.5 V		12	16		12	16	mA
Cin	G and DIR	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 2.5 V or 0.5 V		8			8		pF
<u> </u>	A port	V		18			18		~
Cio	B port	$V_{CC} = 5.5 \text{ V},  V_{I} = 2.5 \text{ V or } 0.5 \text{ V}$		8			8		pF

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.



<sup>‡</sup> For I/O ports, the parameters I<sub>IH</sub> and I<sub>IL</sub> include the off-state output current.

<sup>9</sup> Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

<sup>1</sup> Testing for this parameter on the A port is not recommended.

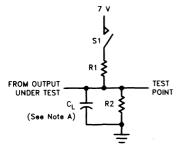
SCBS051 - TI0220 - D3514, MAY 1990 - REVISED SEPTEMBER 1990

## switching characteristics (see Figure 1)

PARAMETER	FROM TO (INPUT) (OUTPUT)		$V_{CC} = 5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = 25^{\circ}C$			V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T <sub>A</sub> = MIN to MAX†				UNIT	
		MIN	TYP	MAX	'54BC	T25245 MAX	MIN	T25245 MAX			
tPLH			1.2	3.3	5.1	1.2	5.8	1.2	5.7		
tPHL	Α	A B	1.9	4.3	6.7	1.9	7.6	1.9	7.2	ns	
t <sub>PLH</sub>	В	В А	1.2	3.3	4.8	1.2	5.7	1.2	5.5		
tPHL			2.1	4	5.6	2.1	6.4	2.1	6.2	ns	
tPZH .	Ğ		3.7	6.3	8.4	3.7	10.1	3.7	9.6		
tPZL		A	4.5	7.4	9.2	4.5	11.1	4.5	10.3	ns	
tPHZ	Ğ		1.8	3.7	5.5	1.8	6.4	1.8	6.2		
tPLZ		A	3.3	5.1	7.2	3.3	9.6	3.3	8.3	ns	
tPZH .	Ğ	ZH S	В	3.4	5.7	7.9	3.4	9.2	3.4	8.9	
tPZL		э В	4.3	6.6	8.7	4.3	10.1	4.3	9.7	ns	
tPHZ	Ğ	Z 0	В	2.7	4.5	6.3	2.7	7.2	2.7	6.9	
t <sub>PLZ</sub>		В	1.7	4.5	6.8	1.7	8.3	1.7	7.5	ns	

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

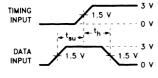
#### PARAMETER MEASUREMENT INFORMATION



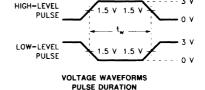
SWITCH POSITION TABLE

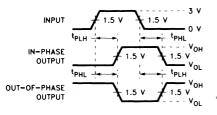
TEST	S1
tpLH	Open
tPHL	Open
tPZH	Open
†PZL	Closed
tPHZ	Open
tPLZ	Closed

LOAD CIRCUIT FOR 3-STATE OUTPUTS

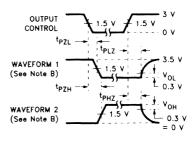


VOLTAGE WAVEFORMS SETUP AND HOLD TIMES





VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLED TIMES, 3-STATE OUTPUTS

NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

  Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. Input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50~\Omega$ ,  $t_f \leq$  2.5 ns,  $t_f \leq$  2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

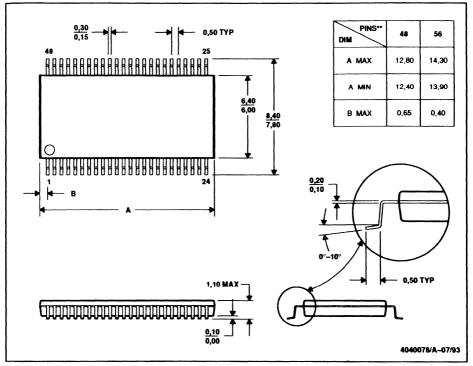


ETL Enhanced Transceiver Logic	1
BTL Backplane Transceiver Logic	2
GTL Gunning Transceiver Logic	3
ABT/CBT 25- $\Omega$ Incident-Wave Switching Drivers	4
Mechanical Data	-



#### DGG/R-PDSO-G\*\*

#### 300-MIL THIN SHRINK SMALL-OUTLINE PACKAGE

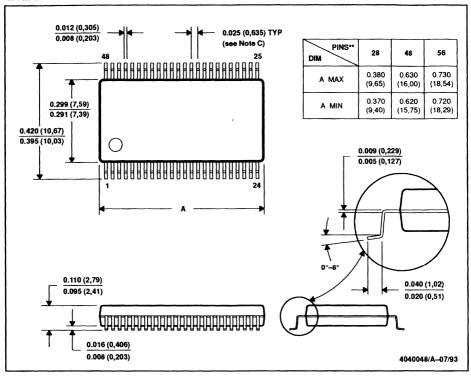


NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions include mold flash or protrusion.

# DL/R-PDSO-G\*\*

#### PLASTIC SHRINK SMALL-OUTLINE PACKAGE



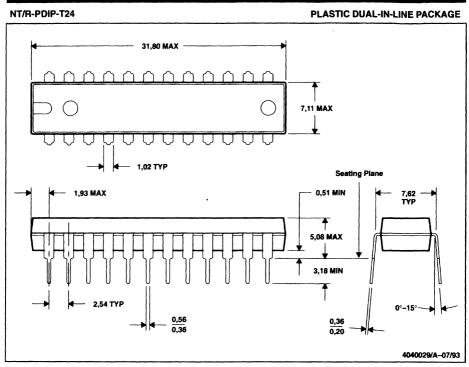
- NOTES: A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Leads are within 0.0035 (0,089) radius of true postion at maximum material condition.
  - D. Body dimensions do not include mold flash , protrusion or gate burn
  - E. Mold flash or protrusion or gate burr shall not exceed 0.015 (0,381).
  - F. Lead tips coplanar within 0.004 (0,102).
  - G. Lead length measured from lead top to point 0.010 (0,254) above seating plane.

#### DW/R-PDSO-G\*\* PLASTIC WIDE-BODY SMALL-OUTLINE PACKAGE 20-PIN SHOWN PINS\*\* 16 20 24 28 0.419 (10,65) DIM 0.400 (10,15) 0.400 0.500 0.602 0.696 A MIN (10, 16)(12,70)(15,29)(17,68)0.297 (7,55) 0.293 (7,45) 0.408 0.508 0.610 0.704 A MAX (10,36)(12,90)(15,49)(17.88)10 0.364 (9,24) 0.338 (8,58) 4° ± 4° 0.104 (2,65) 0.093 (2,35) 0.012 (0,30) 0.012 (0,30) 0.050 (1,27) 0.020 (0,51) 0.004 (0,10) 0.004 (0,10) 0.016 (0,40) 0.014 (0,35) 0.050 (1,27) TYP (see Note C) 4040000/A-07/93

NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. Leads are within 0.10 (0.25) radius of true postion at maximum material condition.
- D. Body dimensions do not include mold flash or protrusion.
- E. Mold flash or protrusion shall not exceed 0.006 (0,15).
- F. Lead tips coplanar within  $\pm 0.004$  ( $\pm 0.10$ ) exclusive of solder.

# **MECHANICAL DATA**

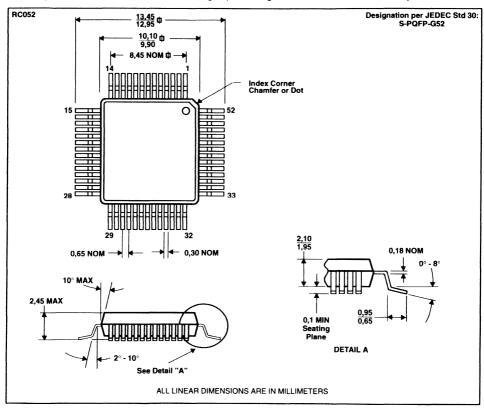


NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Drawing source: SCJ Package handbook, 1990

# RC052 plastic quad flatpack

This plastic package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound withstands soldering temperatures with no deformation, and circuit performance characteristics remain stable when the devices are operated in high-humidity conditions. The package is intended for surface mounting and leads are spaced on 0,65 mm centers with an 0,80-mm foot length. Leads require no additional cleaning or processing when used in soldered assembly.



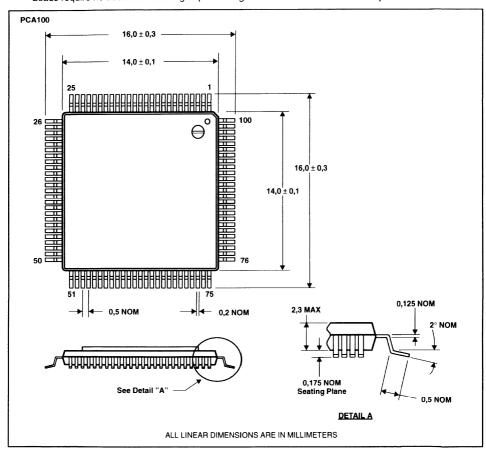
NOTES: A. Maximum deviation from coplanarity is 0,1 mm.

B. All dimensions and notes for JEDEC outline MO-xxxxx apply.

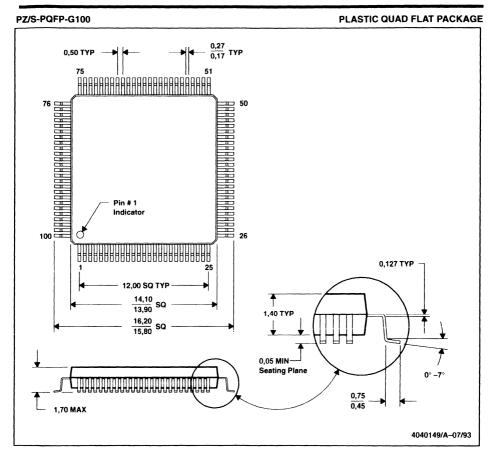


## PCA100 square quad flatpack

This plastic package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperatures with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for surface mounting, and leads are spaced on 1,0-mm centers with a 0,8-mm foot length. Leads require no additional cleaning or processing when used in soldered assembly.







NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Maximum deviation from caplanarity is 0,08 mm.







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